FDL'05

Forum on specification & Design Languages

An ECSI event – co-sponsored by the Swiss Federal Institute of Technology of Lausanne
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Accellera, Cadence, GI, GMM, IEE, IFIP 10.5, ITG, Mentor Graphics, Microswiss Network, Synopsys, VDE, VSIA

September 27 - 30, 2005
EPFL - Lausanne, Switzerland

CALL FOR CONTRIBUTIONS

DEADLINE April 1st, 2005

FDL is the European forum to exchange experiences and learn of new trends in the application of languages and their associated design methods and tools for the design of electronic systems. The forum is organized around thematic areas (TA) (described below) and includes working sessions, poster sessions, embedded tutorials, panels and technical discussions. Fringe meetings such as user group or standardization meetings are also held in conjunction with the forum.

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List can be found in
www.ecsi.org/fdl

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General topics

Specification driven design, formal verification techniques, mixed formal/simulation-based verification techniques, formal languages (B, CTL, Z, temporal logic, etc.), synchronous languages (Esterel, etc.), modeling concepts (e.g. StateCharts, Petri Nets, FSMs, dataflow models, etc.), models of computation.

CSD TA: C/C++-Based System Design

C/C++ for hardware/software system design is entering standard industrial design flows. While SystemC is gaining acceptance for system-level specification and design, Verilog and VHDL are being extended in order to improve their system-level capabilities. This thematic area addresses language-based hardware/software system design and verification methods and tools. Topics include modeling and simulation, performance evaluation and analysis, hardware and software synthesis, RTOS aspects, applications of languages for design verification (CSV, SystemVerilog, etc.), design verification languages (e, PSL/Sugar, etc.), formal and semi-formal methods, etc., requirements to system design and verification languages, interoperability among languages, and roadmaps for the future development of existing approaches.

AMS TA: Analog, Mixed-Signal and Heterogeneous System Design

Heterogeneity of Systems on Chip, and embedded systems is increasing rapidly. Many systems now combine analog/RF, non-electrical (MOEMS) components with digital hardware and an increasing share of software. The combination and tight interaction of continuous and discrete components is still a challenge. Specification, modeling, simulation, (symbolic) analysis, verification, design, (virtual) prototyping or even synthesis of analog, mixed-signal and heterogeneous systems are complex issues. Languages and tools such as, but not limited to, VHDL-AMS, Verilog-AMS, SystemC-AMS, Modelica, or Matlab/Simulink, and formal models like Hybrid Automata are emerging to support such issues from analog circuit design up to system level. The AMS thematic area aims at presenting research activities, practical design experiences, and standardization activities related to these topics.

UML TA: UML-Based System Specification & Design

The Unified Modeling Language supports semi-formal methods for system-level design of complex embedded systems including highly programmable (hardware) platforms and heterogeneous Systems-on-Chip. Current methods do not close the gap from specification to (automatic) synthesis. UML related research topics in this field are Model Driven Development (Model Driven Architecture, platform independent models, platform specific models, and platform description models); design transformations; UML semantics; metamodels (e.g. for SystemC and other System Description Languages and Hardware Description Languages); UML profiles; and formalisation of UML towards domain specific languages for simulation and synthesis. Other topics welcomed are standardisation work; Real-time UML; UML related techniques for performance analysis, validation and verification; SDL; OCL; XMI; and practical design experiences with UML2.

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REQUIREMENTS FOR SUBMISSIONS:

Interested authors are invited to select one submission format from the following list:

- *Short paper format:* A 4-page document that typically describes a work in progress, industrial case studies or users experiences. Accepted short papers will be presented as posters (5 minute presentations during a session and individual discussions during poster display time). Final documents to deliver are a, possibly revised, 4-page document and a poster in A0 or A1 format.
- *Regular paper format:* A 6 to 12-page document that typically goes into more details on innovative and complete research or applicative work with evidence of experimental results. Regular papers may also include new requirements and proposals for standardization. Accepted regular papers will be presented during a time slot of 20 minutes, including 5 minute Q&A.

All papers should be formatted to fit the final format as close as possible, that is A4, one column, min. 2cm left and right margins, single-spaced, Times or equivalent font of minimum 11pt. All papers must include a short abstract and all required figures, tables and references.
The following information is required when submitting a paper:

- *In a separate document:* paper title, name, affiliation, and e-mail address for each author, a designated contact person including his/her phone & fax number, email address, and the concerned thematic area in decreasing order of relevance (keywords are General, AMS, CSD, UML). The document must also include the following statement: "All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the Forum Proceedings and will present the paper at the Forum."
- The submitted paper *without any mention of names and affiliations* to permit a blind review.

See below in the "FORMS OF SUBMISSIONS" box to learn how to submit a paper.
Authors of accepted papers will have to deliver the final version of the papers including recommended changes from reviewers, a copyright release form (which will be provided) and *at least one author registration at the Forum per paper.*

PUBLICATION:

Accepted papers will be included in both electronic (CD-ROM) and printed form to be made available to registered Forum participants. The CD-ROM is published by ECSI and has an ISSN number. It will also include keynote presentations (provided that no confidentiality issues are pending) and tutorial documents. In addition, a selection of best regular papers will be published in an edited book from Kluwer Academic Publishers soon after the event.

TUTORIALS:

Proposals for half-day (4 hours) tutorials on FDL topics will be accepted depending on topic relevance and evidence of a comprehensive agenda. A one page description of the tutorial including title, presenters, contents and the relevant thematic area should be sent to **fdl05@epfl.ch**. A maximum of three tutorial authors is recommended. Accepted tutorials will get one free full registration to the Forum per tutorial.

PANELS, SPECIAL SESSIONS, WORKING GROUPS, PROJECT MEETINGS:

Proposal for special sessions (panels, working sessions, standardization or user group meetings, etc.) around any of the FDL topics are invited and will be accepted depending on their relevance and interest to the audience. They will be embedded in regular workshops. A one page description including title, participants, contents and the relevant thematic area should be sent to **fdl05@epfl.ch**.

DEMONSTRATIONS:

Companies, universities or other organizations providing innovative tools and environments for the topics described above will find in FDL an opportunity to make demonstration of them to the attendees. Proposals should go as soon as possible to the **fdl05@epfl.ch**.

FORMS OF SUBMISSIONS	DEADLINE DATES IN 2005	
Authors are invited to send all information in electronic format through a web submission process (**www.ecsi.org/fdl**).	**Paper submissions due**	**April 01**
In case of problems, please send an email to **fdl05@epfl.ch**.	**Special session & tutorial proposals due**	**April 29**
Accepted electronic formats are in preference order: PDF, OpenOffice, RTF, Postscript.	Notification of acceptance	**June 03**
Compressed submissions are also accepted: GNU gzip, Unix Compress, PKZip.	Final versions of accepted papers due	**July 29**
	Proposal for on-site meetings	**September 02**
	FDL 2005	**September 27-30**

http://www.ecsi.org/fdl

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