DVCon 2004 CALL FOR PAPERS

13th International Conference on Using Hardware Design and Verification Languages

March 1 – 3, 2004
DoubleTree Hotel, San Jose, California, USA
www.dvcon.org

DVCon is the premier conference on the usage of Hardware Description Languages (HDLs), and Hardware Verification Languages (HVLs) for the design and verification of electronic systems and integrated circuits. The focus of the conference is on specialized languages such as VHDL, PSL, Verilog, SystemVerilog, SystemC, SUPERLOG, e and VERA, as well as general purpose languages such as C and C++. Conference attendees are primarily designers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of Electronic Design Automation (EDA) tools. Presentations are highly technical in nature, and reflect real life experiences in using HDLs and HVLs.

TOPIC SUGGESTIONS

Any paper, tutorial or panel related to using HDLs, HVLs or other languages you have used for hardware design or verification will be considered. Here are a few topics that conference attendees might find useful:

- Experiences with top-down or bottom-up system-level design or verification
- Experiences with System-on-Chip design
- Designing and/or verifying FPGAs with embedded processors
- Using multiple HDLs and/or HVLs in a design cycle
- Techniques for directed test, random test, or other verification methods
- Synthesizing high-level languages such as SystemC, System Verilog or C++
- Experiences with hardware/software co-design
- Experiences with mixed-signal simulation
- Verification techniques that really work (and what did not work)
- Successful methods for reducing the time-to-market with electronic engineering projects
- Assertion-based Verification using PSL or other assertion languages (including HDLs)
- Design and Verification IP experiences, good and bad
- Coverage: code, toggle and functional. Measuring completeness and quality of verification
- Formal and Hybrid (dynamic and formal) technologies applied to verification
- Any topic involving the use of an HDL or HVL

We encourage you to contribute your experiences with using hardware design and verification languages, and to participate in the valuable exchange of ideas.

CONFERENCE SCHEDULE:

Monday, March 1
- **Half-day Tutorials am/pm**

Tuesday, March 2 and Wednesday, March 3
- **Opening Keynote Address**
- **Technical sessions**
- **Panel discussions**
- **Exhibits**

SUBMITTING A PROPOSAL - (Opens July 15, 2003)

Proposals must be submitted on-line at www.dvcon.org.

Paper Proposals:

Proposal should be a short abstract of the paper, one to three paragraphs, 300 to 500 words maximum. The abstract must provide enough detail for the program committee to evaluate the technical depth and value of your paper. Be creative with your title!

Panel Proposals:

Proposal should be a short abstract of the panel topic, one to three paragraphs, 300 to 500 words maximum. The proposal should include the proposed Panel members. Please provide enough detail for the program committee to evaluate the technical depth and vaule of your paper.

Tutorial Proposals:

Tutorial proposals should include a description of the topic and a lesson plan or outline of your class. Proposals should include all the presenters that will be teaching the class.

AUTHOR'S SCHEDULE:

- **October 1, 2003:** Paper, tutorial and panel proposals due
- **October 31, 2003:** Acceptance notification for all types
- **December 12, 2003:** Complete review draft of papers due
- **January 15, 2004:** Final paper due to proceedings printer
- **February 12, 2004:** Tutorial handouts due

FINAL PUBLICATION REQUIREMENTS

If your proposed paper is accepted, an author kit with details on paper formatting will be sent to you. Final papers should be between 4 and 8 pages, two-column, single-spaced. Final tutorial materials should include a copy of all presentation slides.

SPONSORED BY

The Design and Verification Conference, DVCon, is sponsored by Accellera, www.accellera.org. Accellera is an industry consortium dedicated to the development and standardization of design and verification languages.

For more information concerning the conference, please contact the conference management:

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