

Prioritization Polling Results												
	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	Total	Voters
XMR	7	1	1	2	1	2	1	2	1	1	11	Bhasker, Lewis, Ajay, Deepak, Hsu, Perry, Ostler, Thompson, Martinolle, Anderson, Sforza
Direct C & Verilog calls / std IF Text IO	5	2	1	2	1	2	1	2	1	1	11	Bishop, Lewis, Lavelle, Ajay, Deepak, Hsu, Perry, Kumar, Thompson, Sforza
to_string-type capabilities	7	2	1	1	1	1	1	1	1	1	10	Bhasker, Munden, Lewis, Bishop, Lavelle, Hsu, Perry, Ashenden, Myers, Sforza, Goeke
Allow reading of out mode ports	3	2	2	1	1	1	1	1	1	1	10	Ries, Myers
Performance Assertions	4	2	2	2	1	1	1	1	1	1	9	Ries, Bishop, Perry, Kumar, Anderson, Myers, Sforza, Peterson
Apply Accellera Assertions	4	1	1	1	1	1	1	1	1	1	9	Moretti, Ries, Willis, Bailey, Lavelle, Ajay, Deepak, Sforza, Peterson
Case statement expressions (choices)	3	1	1	1	1	1	1	1	1	1	3	Ries, Bishop, Thompson
More locally static exprs; local/global cleanup	2	1	1	1	1	1	1	1	1	1	5	Swart, Bishop, Lewis, Perry, Kumar, Goeke
Don't care in case stmts and compares	1	1	1	2	1	1	1	1	1	1	5	Swart, Kumar, Ostler, Guyler, Martinolle, Goeke, Peterson
VCD for VHDL	1	1	1	2	1	1	1	1	1	1	5	Ries, Ajay, Deepak, Martinolle, Anderson
Simulation control subprograms	3	2	1	1	1	1	1	1	1	1	5	Bishop, Lewis, Martinolle, Myers
elseif/elsif clause in generate	2	1	1	1	1	1	1	1	1	1	4	Bishop, Ostler, Thompson, Anderson, Peterson
Data types & abstractions	2	1	1	1	1	1	1	1	1	1	4	Ashenden, Shields, Martinolle, Anderson, Peterson
Testbench/VeriCOO	1	1	1	2	1	1	1	1	1	1	4	Moretti, Willis, Lavelle, Hsu, Peterson
Read & sim Verilog netlist	1	1	1	2	1	1	1	1	1	1	4	Williams, Bishop, Lewis
Eliminate guarded blocks & signals					3	1					4	Williams, Kumar, Ashenden
Image values	3	1	1	1	1	1	1	1	1	1	3	Munden, Ashenden, Thompson, Peterson
Eliminate everything marked for deprecation	2	1	1	1	1	1	1	1	1	1	3	Williams, Bishop, Anderson
Regularized & minimized bracketing (end)	2	1	1	1	1	1	1	1	1	1	3	Bhasker, Bishop, Williams, Kumar
Load/dump memories	2	1	1	1	1	1	1	1	1	1	3	Kumar, Ostler, Guyler, Peterson
Integrate 1164, 1076.x	2	1	1	1	1	1	1	1	1	1	3	Lavelle, Kumar, Thompson
Eliminate type conversions where possible	2	1	1	1	1	1	1	1	1	1	3	Williams, Lavelle, Perry
Conditional analysis & macros	2	1	1	1	1	1	1	1	1	1	3	Ostler, Ashenden, Martinolle
Identify processes as combinatorial	2	1	1	1	1	1	1	1	1	1	3	Bailey, Hsu, Shields
Modeling & User Productivity	1	1	1	1	1	1	1	1	1	1	3	Ries, Thompson, Guyler, Goeke
Expressions in port maps	1	1	1	2	1	1	1	1	1	1	3	Ries, Lavelle, Martinolle
Associative arrays	1	1	1	2	1	1	1	1	1	1	3	Hsu, Martinolle, Anderson
Implicit generic/port map in comp instance sync/hand-shaking; request action/wait action	1	1	1	1	1	1	1	1	1	1	3	Bhasker, Ostler, Lewis
Expressions in sensitivity list											3	Ajay, Deepak, Myers, Goeke
User-defined real mantissa/exponent											2	Williams, Bishop
Constraining size of hex, octal, dec values											2	Bishop, Lewis
case generate											2	Bishop, Thompson
Bi-directional connections (jumpers, switch)											2	Munden, Bishop

