VASG Kicks-Off VHDL 200x

Stephen Bailey
Chair

Your Design Partner

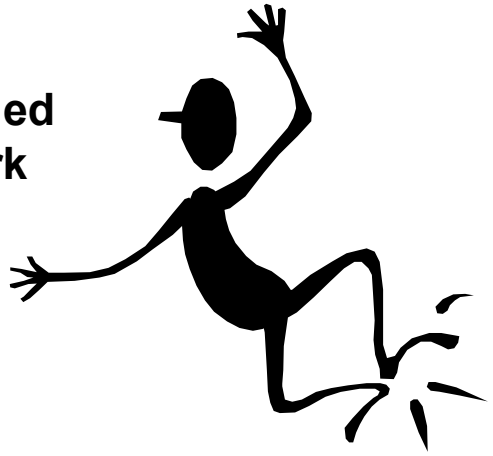
SYNOPSYS®

Agenda

- Welcome
- SA Boilerplate
- Review of Tuesdays Public Meeting
- What we are doing today
- What we are NOT doing today
- The Process
- Schedule & Next meeting(s)

Welcome!

- **I'm pleased by the interest in the future of VHDL!**
- **After a few false starts**
  - **I am glad to report that I am actually being pushed by others to get this work moving and on track!**



Instructions for the WG Chair (Not necessary to be shown)

- At Each Meeting, the Working Group Chair shall:
- Show slides #1 and #2 of this presentation
- Advise the WG membership that:
  - **The IEEE's Patent Policy is consistent with the ANSI patent policy and is described in Clause 6 of the *IEEE SA Standards Board Bylaws*;**
  - **Early disclosure of patents which may be essential for the use of standards under development is encouraged;**
  - **Disclosures made of such patents may not be exhaustive of all patents that may be essential for the use of standards under development, and that neither the IEEE, the WG nor the WG Chairman ensure the accuracy or completeness of any disclosure or whether any disclosure is of a patent that in fact may be essential for the use of standards under development.**
- Instruct the WG Secretary to record in the minutes of the relevant WG meeting:
  - **that the foregoing advice was provided and the two slides were shown;**
  - **that an opportunity was provided for WG members to identify or disclose patents that the WG member believes may be essential for the use of that standard;**
  - **any responses that were given, specifically the patents and patent applications that were identified (if any) and by whom.**

Approved by IEEE-SA Standards Board – December 2002

IEEE-SA Standards Board Bylaws on Patents in Standards Slide #1

6. Patents

IEEE standards may include the known use of patent(s), including patent applications, provided the IEEE receives assurance from the patent holder or applicant with respect to patents essential for compliance with both mandatory and optional portions of the standard. This assurance shall be provided without coercion and prior to approval of the standard (or reaffirmation when a patent becomes known after initial approval of the standard). This assurance shall be a letter that is in the form of either

a) A general disclaimer to the effect that the patentee will not enforce any of its present or future patent(s) whose use would be required to implement the proposed IEEE standard against any person or entity using the patent(s) to comply with the standard or

b) A statement that a license will be made available without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination

This assurance shall apply, at a minimum, from the date of the standard's approval to the date of the standard's withdrawal and is irrevocable during that period.

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Inappropriate Topics for IEEE WG Meetings Slide #2

- **Don’t discuss licensing terms or conditions**
- **Don’t discuss product pricing, territorial restrictions or market share**
- **Don’t discuss ongoing litigation or threatened litigation**
- **Don’t be silent if inappropriate topics are discussed… do formally object.**

If you have questions,
contact the IEEE Patent Committee Administrator
at patcom@ieee.org

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Review of Public Meeting

- On Tuesday, we held a public meeting at DVCon
- Purpose: Publicize our work to update VHDL
- Well attended at least 15 people
- Good reception
- Concerns about tool support
  - All depends on user demand
  - If we do the right things
  - Users will demand it

Review of Public Meeting

- Recommended
  - We do 1st cut prioritization today
  - Review that prioritization next week at DATE
  - Adjust priorities, if needed
  - Publish priorities more broadly

What are we doing today?

- This is an organizational meeting
- Agree on process
- Agree on initial break-out of functional responsibilities
- Identify the functional team leaders
- Identify initial priorities
- Identify and schedule key milestones
  - We will ship on schedule!

What We are NOT Doing Today

- We are not here to gather additional or analyze requests (beyond prioritization)
  - You can submit your requests via the bugs and enhancements link at: http://www.eda.org/vasg
- Requests will be analyzed and resolved by functional teams (to start following this meeting)
  - For details on joining these teams:
    - vhdl-200x@eda.org or stephen@srbailey.com
    - http://www.eda.org/vasg (coming soon)

The Process

- Standards are not a process where you get everything you want.
  - Standards are a consensus process where everyone gets something they can live with.
- Issues and disagreements will be resolved by consensus.
  - Chair is a moderator, not a dictator
  - Additional process rules will be formulated on an as needed basis.
- Participants are expected to be reasonable professionals during this process

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The Process

- Collect requests
- Reasonableness check & assignment
- Analyze request & prioritize
- Propose language change
- Review change
- Integrate change
- Update LRM
- Ballot & Publish
- Repeat (as needed)

The Process

- Validation
  - Software Prototype (preferred)
    - EDA vendor(s) prototyped the change
    - At least one end user has tested the change
  - Paper Prototype
    - Technical work completed
    - User provided tests & examples
  - WG approves all validated changes

Accellera & IEEE

- IEEE owns the copyright to VHDL
  - Therefore, official standardization via IEEE standards balloting process
- Accellera
  - Facilitates: Resources, coordination and publicity
  - Can facilitate announcing and making available intermediate drafts and milestones of the WG

Fast-Tracking

- Can (should) we fast-track a limited set of capabilities?
  - 1164 and 1076.3 could use:
    - vector/scalar logical operations
    - unary reduction operations
    - Possibly to_string or similar IO formatting
  - Standard Signal Spy / XMR capability
- I think we should try to meet their needs ASAP

Teamwork

- Must divide the work to make timely progress
  - How many teams?
  - Scope for each team?
  - Resolving overlaps?
  - Reviewing team findings and recommendations
  - Integrating team results into a coherent whole
- But WG can direct priorities

For each team

- Enumerate initial assignment of requests
- Also, want to allow the flexibility that more than one team can analyze the same request
  - Require both (all) teams to agree to proposed (re)solution
- Team members and team leader

Proposed Teams

- Steering Committee (S Bailey)
- Fast-Track (J Lewis or J Willis)
- Simulation performance (J Ries)
- Assertions (R Anderson)
- Testbench/verification (J Bhasker)
- Environment (D Soderberg)
- Modeling and productivity (J Lewis)
- Data types and abstraction (P Menchini)
- Miscellaneous (J Willis)

Steering Committee

- Scope/responsibility
  - Delegate requests
  - Coordinate / integrate technical work
- Chaired by VASG Chair
- Membership:
  - All team leaders (including ISAC chair)
  - Others if nominated by Chair and approved by SC
    - Dennis Brophy: Accellera Liaison

Fast-Track

- Scope / responsibilities
  - Support related standards (1164, 1076.x)
  - Quick resolution of key requests
- Chair
  - John Willis & Jim Lewis (co-chairs)
  - jwillis@ftlsys.com
  - jim@synthworks.com

Fast-Track (2)

- Initial assignment:
  - vector/scalar logical operations
  - unary reduction operations
  - Possibly to_string or similar IO formatting
  - Standard Signal Spy / XMR capability

Simulation Performance

- Scope / responsibilities
  - Language changes that facilitate enhanced tool performance
  - Primarily, but not only, simulation
- Chair
  - John Ries
  - johnr@model.com

Simulation Performance (2)

- Non-blocking assignment / light-weight signals (0-delay)
- Remove delta cycles
- Identify processes as combinatorial
- posedge / negedge; expressions in sensitivity lists
- 2 & 4 state semantics
- Elimination of guarded blocks and signals
- User control of signal atomicity
- Eliminate everything marked for deprecation in 2002
- Eliminate inc port binding, groups, pulse-reject limit
- Optional ignore / use of size of real numbers

Assertions

- Scope / responsibilities
  - Define support for temporal expressions and assertion-based verification in VHDL
  - Exploit work of others
  - Consider formal, synthesis and coverage implications
- Chair
  - Rob Anderson
  - rob@reawebtech.com

Assertions (2)

- Temporal expressions
- Allow reading of output ports
- orif, orels, errels for expressing mutual exclusivity to specify (one-hot?) assertion
- Apply Accellera assertions to VHDL
- Assertion severity mapped to breakpoint
- Relationship of assertions to coverage and TB reactivity

Testbench / Verification

- Scope / responsibilities
  - Language enhancements that ease the job of the verification engineer
  - Modeling DUV environment and I/O
  - Consider coverage and assertions implications
- Chair
  - J Bhasker
  - bhasker@esilicon.com

Testbench / Verification (2)

- Improved formatted Text IO (yes overlap with Fast-track)
- assigned image values for identifier-based enumerated type values
- fork/join/pipeline; dynamic process creation/destruction (overlap with modeling & productivity)
- Sync and handshaking
- Request action / wait for action
- Expected value detectors
- Access to coverage data (VhPI) for reactive TB
- XMR (hierarchical signal reference)
- Sparse arrays (overlap type system)

Testbench / Verification (3)

- Associative arrays (overlap with type system)
- Queues/FIFOs (possible overlap with type system)
- Object-orientation (overlap with type system)
- Random value generation w/ optional & dynamic weighting
- Random object initialization
- Random 2 state value resolution in place of X generation
- Random choice selection w/ optional & dynamic weighting
- Loading & dumping memories

Environment

- Scope / responsibilities
  - Simulation control environment
  - Standard interfaces to other languages
  - Additional support packages
- Chair
  - Dennis Soderberg (?)
  - dennis@ftlsys.com

Environment (2)

- Read & simulate Verilog gate netlists
- Verilog and C Foreign interfaces
- Direct C and Verilog calls
- Simulation control subprograms (like $stop, etc. in Verilog)
- Assertion severity mapped to breakpoint (overlap with assertions)
- Extended HW functions like DW (mux, decoders, adders)
- Tool-specific constants
- Macros
- Conditional compilation

Environment (3)

- VCD for VHDL
- Multiple hierarchy roots
- Library mappings standardize the specification
- TEE functionality to STD.OUTPUT
- Forcing values/strong values

Modeling & Productivity

- Scope / responsibilities
  - Improve designer productivity through
    - Enhanced conciseness
    - Accurate intent capturing
    - Simplifying common occurrences of code
  - Enhance VHDL to allow (easy) modeling of functionality current difficult or impossible
- Chair
  - Jim Lewis
  - jim@synthworks.com

Modeling & Productivity (2)

- Allow concurrent sig asmt in sequential code
- Array aggregates on LHS (alternative to concat on LHS
- Value folding of std_ulogic (2 state/4 state)
- Case statement expressions (choices)
- More locally static exprs (concatenation, index and slicing of static objects/values)
- Make transport the default delay mode
- rising/falling edge for bit
- Bit_vector has unsigned interpretation
- Bidirectional connections (simple switch, jumper)
- Remove white space requirement in physical literals

Modeling & Productivity (3)

- Allow “;” to terminate as well as separate interface lists
- Regularized & minimized bracketing (end)
- Subp bodies in package declarations
- else/elsif clause in if-generate
- case generate
- endif (like elsif)
- orif, orels, etc for mutual exclusive FSM
- Comparisons (logic ops) that return std_ulogic
- Attribute declarations in code space (not just decl part)
- Expressions mapped to ports with events
- Longest static prefix issue with loops
- Don’t cares in case statements and compares

Modeling & Productivity (4)

- Non-locally static expressions in case statements
- Short alias name for std_logic_vector
- Boolean equivalence (short-hand for equivalencing typed expressions, eg. if sl then)
- Integrate 1164, 1076.2, 1076.3 into 1076
- Eliminate passive statement restriction on entities
- Ability to apply register kind semantics to std_logic (retain last resolved value when all drivers off)
- Implicit generic/port map in component instance
- Dynamic process create/destroy to model reconfig HW (overlap with TB/verification)

Data Types & Abstraction

- Scope / responsibilities
  - Enhancements centered on the type system (variant records/unions, OO)
  - Higher abstraction level constructs (interfaces)
- Chair
  - Paul Menchini
  - mench@mench.com

Data Types & Abstraction (2)

- Constraining size of hex, octal and decimal values/objs
- Greater than 32-bit range for integers (infinite range)
- Record templates with unconstrained fields
- Variant records / unions with bit-level mapping
- Bit operations (recognized bit representation of all types/values)
- Eliminate type conversions whenever possible
- Fixed point types (user-defined precision, etc)
- User-defined floating point mantissa/exponent
- Garbage collection of access types
- Sparse & associative arrays (overlap Verification/TB)
- Ragged arrays (like record templates)

Data Types & Abstraction (3)

- User-defined default initial value for (sub)types (overlap with TB/verification if allow (weighted) random initial values)
- User-defined positional values of enum literals
- Interface construct supporting multiple abstraction levels
- Object-orientation (overlap Verification / TB)
- User control over signal atomicity (overlap Performance)
- Named events (data-less signals) (move to verification/TB)

Initial Priorities

- There are ~100 items listed in previous slides.
- Prioritization process:
  - Everyone pick their top 10 requests
  - Can identify entire category (e.g., makes most sense for Assertions and Performance, but no restriction)
  - Initial priority will be according to number of top 10 votes received

Initial Priorities

- We will float this set of initial priorities at DATE next week
- We will adjust, if needed, based on feedback from DATE attendees
- Then we will do a final check via broad publication of priorities (comp.lang.vhdl, web site)
- Any WG top priorities will be top priorities within each technical team

Additional Priorities

- **After WG priorities are satisfied**
  - **Each team may prioritize remaining requests within their scope**
  - **Attack each in priority order**
- **That is, technical team is not finished just because top WG priorities in their area are complete**
  - **They can do as much as they have time to do**

Schedule

- **DATE**
  - **Informational meeting (like DVcon mtg)**
- **DAC**
  - **Each team has:**
    - **Technical direction on all WG top priority items**
    - **Identification of additional team priorities**
    - **Schedule to achieve draft 1**
      - Must include WG top priority items
  - **DAC+1 Fast-track has:**
    - **Technical proposal submitted for WG review and approval**

Schedule

- DAC+2 month
  - WG determination of fast-track update
  - Will it be submitted for balloting?
- Dec 03
  - Draft 1 submission to VASG for approval
    - May or may not be submitted for IEEE balloting
    - WG needs to decide if IEEE approval at that time is a good use of time
    - Clearly some relationship to fast-track
  - Anything fast-tracked is done (ballot finishing)

Schedule

- DAC 04
  - Draft 2 submission to WG for review/approval
  - Assumed this draft will be balloted
    - WG to make final IEEE balloting determination
  - WG assessment of remaining work
    - Development of continued work plan
    - Including additional drafts
    - IEEE balloting
- End '04
  - Complete ballot of draft 2

Schedule

- Steering Committee
  - WG Chair, ISAC Chair, team leaders
  - Review progress fortnightly or monthly
- Teams
  - Must meet no less frequently than fortnightly to ensure progress
  - Assume virtual meetings (telecon/web)
    - Up to team to decide most effective way to meet

Next Meetings

- DATE
  - Summary of this meeting
  - Combined with DVCon public info
- SC
  - 14 or 18 March via telecon
    - Ensure all teams have started
    - Check on infra/support needs
  - 8 Apr via telecon
    - Review initial priority lists
    - Fast-track: Go/no-go; dependencies

Next Meetings

- **Next face-to-face?**
  - **DAC ‘03?**
  - **Other?**