VHDL 04 Language Revision

25 Feb 03

Stephen Bailey
Chair, IEEE 1076 Working Group
(VHDL Analysis and
Standardization Group -- VASG)

Agenda

- **Why a language revision now?**
- **What can we expect to see?**
- **Who will be doing the work?**
- **How can I get involved?**
- **Panel: Q&A with audience**

Why a language revision now?

- **VHDL has been very stable since 1993**
  - **VHDL users have found the language provides most of what was needed for RTL design and verification**
- **But progress overtaking stability**
  - **Design sizes**
  - **Especially explosion in verification cycles**
  - **New methods becoming state-of-practice**
- **Revise VHDL for methods and productivity**

What can we expect to see?

- **Design and verification productivity**
  - **Shorter, more concise designs and testbenches**
  - **Faster tools**
- **Testbench/Verification**
- **Higher abstraction levels**
- **General functional improvements**
- **Simplifications**

The Fine Print

- **In the following slides:**
    - **Many requests are covered**
    - **This is not comprehensive**
    - **It is only a sample**
    - **There is no guarantee of new features**
    - **Only a promise that we will do at least a 1st level analysis of all requests**

Design & Verification Productivity

- **Faster tool performance**
    - **Eliminate anachronisms (linkage)**
    - **New features to key tool optimizations**
    - **Changes to facilitate tool optimizations (delta cycle collapse)**
- **Designer/Verifier productivity**
    - **Low level access from abstract types**
    - **Features/short-hand for common ops**
    - **Conciseness & accuracy in design intent**
    - **Relax/rationalize use restrictions**

Type System / Abstraction

- **User-defined bit-layout of types**
    - **Integers (including >32 bits)**
    - **User-defined floating point/fixed point**
    - **Enumerations**
    - **Records**
- **Unions / variant records**
- **Object-orientation**
- **Sparse / associative arrays**
- **Interface objects**

Verification & TestBenches

- **Assertion-based verification support**
- **Formatted textio and string ops**
- **High-level communications (mailboxes & queues)**
- **Random data gen and alternative selection**
- **XMR/Signal spy**
- **Dynamic process creation/deletion**
- **Coverage data collection & access**

Modeling Capabilities

- **"Register-kind" applied to std_logic**
- **Additional operations**
  - **Vector/scalar logical ops**
  - **Unary reduction**
- **"Pass-thru" gate (jumpers)**
- **Garbage collection**
- **case-generate and if-else generate**

Environment

- **Direct C and Verilog**
- **Standard sim control commands & subprograms**
- **VCD for VHDL**
- **Conditional analysis (predefined "macros")**

What can we expect to see? Process

- **Leveraging of industry efforts**
  - **Keep implementation costs lower**
- **Strive for simplicity in design**
  - **Higher performance & quality tools**
  - **Easier to learn**
- **Keep to VHDL style and nature**
- **Commitment from EDA vendors**
- **Interactive validation from end-users**
- **Backward compatibility**

11

Fast-Tracking

- **Phased release/approval of capabilities**
  - **WG defined approved, unofficial version**
- **Some limited capabilities could be fast-tracked**
  - **Relatively non-controversial**
  - **Local language impact**
  - **Benefits other dependent standards**
    - **Vector/scalar logical ops**
    - **Unary reduction**
    - **???**

12

Who will be doing the work?

- **IEEE is the standards organization (VASG & SA)**
- **Accellera will provide resources and logistics to assist**
- **But, ultimately:**
  - **EDA vendors & highly motivated individuals**
  - **Driven by end-user needs**
  - **As reflected in the active participation in VASG**

Organization

- **Time-honored: Divide and conquer**
  - **ISAC (standing subcommittee of VASG)**
    - **Will review all inputs and delegate/assign**
  - **Technical committees will be formed**
    - **Based on common functional / technical areas**
  - **VASG will coordinate the committees**
    - **Overlaps will happen**
    - **Broader reviews and integration of effort required**

Process

- **Collect requests and inputs (on-going)**
- **Form committees with defined scopes**
- **Committees**
  - **Identify end-user drivers**
  - **Identify priorities**
  - **Perform analysis and technical work**
  - **Submit work at discrete points for VASG and broader review**

Process (2)

- **EDA Vendors (overlapping roles)**
  - **Help identify end-user**
  - **Prototype proposed changes**
  - **Solicit validation of prototypes from end-user**
  - **Provide feedback on implementation difficulty and validation results**

Process (3)

- **VASG**
  - **Herd the committees**
  - **Ensure all work integrates**
  - **Ensure all work keeps VHDL consistent**
  - **Ensure all work is properly reviewed**
  - **Ensure all significant language changes have been validated by end-users and have at least one sponsoring EDA vendor**
  - **Update LRM and ballot revised standard**

How can I get involved?

- **All IEEE standards efforts are open**
- **VASG and committees define membership**
  - **Generally, WG/committee activity required**
  - **Anyone can monitor & review results**
  - **DASC membership ($40 or $50)**
- **For balloting, must be IEEE SA member**
  - **IEEE member + $10 for SA membership**
    - **Case-by-case exceptions possible**

How can I get involved? (2)

- **Subscribe:**
  - **majordomo@eda.org: vhdl-200x**
  - **Post privileges: controlled by VASG chair (sbailey@synopsys.com or stephen@srbailey.com)**
- **Contact any of the individuals on the panel or the chair and let us know your interest**

How can I get involved? (3)

- **How can I submit requests?**
- **http://www.eda.org/pub/vasg/**
  - **Click on bugs&enhancements link**
  - **Fill out the form to the best of your ability.**
- **We may modify the submission process**
  - **If we do, the eda.org/pub/vasg page will provide directions/links**

Panel Q&A

Ask any question you want or any comments

We will do our best to provide an answer or record the information

John Ries
Jim Lewis
John Willis?
Dennis Brophy?
Alex Zamfirescu?