

# P1076

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**Submitter Email:** jim@synthworks.com

**Type of Project:** Revision to IEEE Standard 1076-2008

**PAR Request Date:** 29-Nov-2010

**PAR Approval Date:**

**PAR Expiration Date:**

**Status:** Unapproved PAR, PAR for a Revision to an existing IEEE Standard

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**1.1 Project Number:** P1076

**1.2 Type of Document:** Standard

**1.3 Life Cycle:** Full Use

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**2.1 Title:** Standard for VHDL Language Reference Manual

**Old Title:** IEEE Standard VHDL Language Reference Manual

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**3.1 Working Group:** VHDL Analysis and Standardization Group (C/DA/P1076)

**Contact Information for Working Group Chair**

**Name:** Jim Lewis

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**Contact Information for Working Group Vice-Chair**

**Name:** Charles Swart

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**3.2 Sponsoring Society and Committee:** IEEE Computer Society/Design Automation (C/DA)

**Contact Information for Sponsor Chair**

**Name:** Stanley Krolikoski

**Email Address:** skrolikoski@gmail.com

**Phone:** 925-336-9343

**Contact Information for Standards Representative**

None

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**4.1 Type of Ballot:** Individual

**4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot:** 07/2014

**4.3 Projected Completion Date for Submittal to RevCom:** 10/2014

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**5.1 Approximate number of people expected to be actively involved in the development of this project:** 30

**5.2 Scope:** This project revises and enhances the VHDL language reference manual (LRM) by adding general language enhancements in the areas of design and verification of electronic systems.

**Old Scope:** his standard revises and enhances the VHDL language reference manual (LRM) by including a standard C language interface specification; specifications from previously separate, but related, standards IEEE Std 1164 -1993,1 IEEE Std 1076.2 -1996, and IEEE Std 1076.3-1997; and general language enhancements in the areas of design and verification of electronic systems.

**5.3 Is the completion of this standard dependent upon the completion of another standard:** No

**5.4 Purpose:** The VHDL language was defined for use in the design and documentation of electronics systems. It is being revised to incorporate capabilities that improve the language's usefulness for its intended purpose as well as extend it to address design verification methodologies that have developed in industry. These new design and verification capabilities are required to ensure VHDL remains relevant and valuable for use in electronic systems design and verification.

**Old Purpose:** The VHDL language was defined for use in the design and documentation of electronics systems. It is revised to incorporate capabilities that improve the language s usefulness for its intended purpose as well as extend it to address design verification methodologies that have developed in industry. These new design and verification capabilities are required to ensure VHDL remains relevant and valuable for use in electronic systems design and verification. Incorporation of previously separate, but related standards, simplifies the maintenance of the specifications.

**5.5 Need for the Project:** General language enhancements improve designer productivity by allowing the specification of models more efficiently or the ability to specify functionality that was previously not possible or impractical to specify in VHDL. Verification capabilities are needed to improve the quality of the designs and to address the significant and growing portion of the electronic system design schedule that is being spent in ensuring the design is functionally correct before manufacturing. These capabilities directly address productivity and quality.

**5.6 Stakeholders for the Standard:** - Digital IC and FPGA IP developers  
- Digital IC and FPGA developers and manufacturers  
- Digital and embedded system developers, manufacturers and integrators,  
- Electronics Design Automation (EDA) tool vendors

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### Intellectual Property

**6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?:** No

**6.1.b. Is the Sponsor aware of possible registration activity related to this project?:** No

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**7.1 Are there other standards or projects with a similar scope?:** Yes

**If Yes please explain:** There are 3: IEEE 1364 (Verilog), IEEE 1647 (e), and IEEE 1800 (System Verilog).

There is overlap between the capabilities of these languages, however, VHDL has been proven in the market and multiple tools currently support it.

**and answer the following**

**Sponsor Organization:** IEEE/DASC

**Project/Standard Number:** P1800

**Project/Standard Date:** 01-Jan-2009

**Project/Standard Title:** IEEE 1364 (Verilog): Standard for Verilog Hardware Description Language.

IEEE 1647 Standard for the Functional Verification Language 'e':

IEEE 1800 Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language.

**7.2 Joint Development**

**Is it the intent to develop this document jointly with another organization?:** No

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**8.1 Additional Explanatory Notes (Item Number and Explanation):**