P1666.1

Submitter Email: skrolikoski@gmail.com
Type of Project: New IEEE Standard
PAR Request Date: 01-Oct-2013
PAR Approval Date: 11-Dec-2013
PAR Expiration Date: 31-Dec-2017
Status: PAR for a New IEEE Standard

1.1 Project Number: P1666.1
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: SystemC Analog/Mixed-Signal (AMS) extensions Language Reference Manual

3.1 Working Group: SystemC AMS extensions Working Group (C/DA/P1666.1)
Contact Information for Working Group Chair
Name: Martin Barnasconi
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Contact Information for Working Group Vice-Chair
None

3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)
Contact Information for Sponsor Chair
Name: Stanley Krolikoski
Email Address: skrolikoski@gmail.com
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Contact Information for Standards Representative
None

4.1 Type of Ballot: Entity
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 01/2014
4.3 Projected Completion Date for Submittal to RevCom: 10/2014

5.1 Approximate number of entities expected to be actively involved in the development of this project: 12
5.2 Scope: This standard defines the Analog/Mixed-Signal extensions for SystemC, as an ANSI standard C++ class library for system and hardware design including analog/mixed-signal elements.

5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: The general purpose of the SystemC AMS extensions is to provide a C++ standard for designers and architects, who need to address complex heterogeneous systems that are a hybrid between hardware and software. This standard is built on the IEEE Std 1666-2011 (SystemC Language Reference Manual) and extends it to create analog/mixed-signal, multi-disciplinary models to simulate continuous-time, discrete-time, and discrete-event behavior simultaneously.
The specific purpose of this standard is to provide a precise and complete definition of the AMS class
Library, so that a SystemC AMS implementation can be developed with reference to this standard alone.
This standard is neither intended to serve as a user's guide nor to provide an introduction to AMS extensions in SystemC, but does contain useful information for end users.

5.5 Need for the Project: As the electronics industry builds more complex systems involving large numbers of components including analog/mixed-signal and software content, there is an increasing need for a system-level design language that can manage the complexity and size of these embedded systems. The SystemC AMS extensions provide efficient mechanisms to describe the analog and mixed-signal properties of these systems at higher levels of abstraction. These capabilities are not available in traditional hardware description languages. The SystemC AMS 1.0 standard has been released by the Open SystemC Initiative in 2010, and the updated AMS 2.0 standard in March 2013 by the successor organization Accellera Systems Initiative, making it a mature EDA standard.

5.6 Stakeholders for the Standard: Stakeholders for this project are Electronic Design Automation (EDA) companies that implement the technology, Integrated Circuit (IC) suppliers who use the technology, and end users who build systems based on the technology.

Intellectual Property
6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: Yes
If yes please explain: A copyright transfer letter will be required from the Accellera Systems Initiative. Accellera Systems Initiative has indicated that they will provide such a letter.

6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

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7.1 Are there other standards or projects with a similar scope?: Yes
If Yes please explain: There are two other standards addressing analog/mixed-signal extensions for hardware description languages:
- Verilog-AMS 2.3.1, an Accellera Systems Initiative standard, released 6/1/2009.
- IEEE Std 1076.1 (also known as VHDL-AMS), approved in 1999 and revised in 2007.
Although these standards provide similar analog and mixed-signal modeling capabilities, their primary intent is to address AMS modeling at the circuit and physical implementation level. The SystemC AMS extensions more focus on the system-level modeling aspects, by introducing a more abstract modeling style based on data flow semantics. This is neither covered in Verilog-AMS nor in VHDL-AMS.

and answer the following
Sponsor Organization: Accellera Organization, Inc.
Project/Standard Number: Verilog-AMS 2.3.1, IEEE Std 1076.1-2007
Project/Standard Date:
Project/Standard Title: Verilog-AMS Language Reference Manual and
Standard VHDL Analog and Mixed-Signal Extensions
7.2 Joint Development
Is it the intent to develop this document jointly with another organization?: No

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8.1 Additional Explanatory Notes (Item Number and Explanation): Information for 7.1:
IEEE 1076.1-2007 is titled "IEEE Standard VHDL Analog and Mixed-Signal Extensions". However the IEC dual logo standard published in 2009 (listed as both as IEC 61691-6 and IEEE 1076.1) is titled "Behavioural languages - Part 6: VHDL Analog and Mixed-Signal Extensions".