**P1647**

**Submitter Email:** darren.galpin@infineon.com
**Type of Project:** Modify Existing Approved PAR
**PAR Request Date:** 11-Sep-2012
**PAR Approval Date:**
**PAR Expiration Date:**
**Status:** Unapproved PAR, Modification to a Previously Approved PAR for the Revision of a Standard

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| **Root PAR:** P1647 |  **Approved on:** 19-Nov-2010 |

**1.1 Project Number:** P1647
**1.2 Type of Document:** Standard
**1.3 Life Cycle:** Full Use

**2.1 Title:** Standard for the Functional Verification Language 'e'

**3.1** **Working Group:** Functional Verification Language e Working Group (C/DA/eWG)
**Contact Information for Working Group Chair**
   **Name:** Darren Galpin
   **Email Address:** darren.galpin@infineon.com
   **Phone:** 44 (0)117 9528741
**Contact Information for Working Group Vice-Chair**
None

**3.2** **Sponsoring Society and Committee:** IEEE Computer Society/Design Automation (C/DA)
**Contact Information for Sponsor Chair**
   **Name:** Stanley Krolikoski
   **Email Address:** skrolikoski@gmail.com
   **Phone:** 925-336-9343
**Contact Information for Standards Representative**
None

**4.1 Type of Ballot:** Individual
**4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot:** 01/2014
**4.3 Projected Completion Date for Submittal to RevCom:** 02/2014

**5.1 Approximate number of people expected to be actively involved in the development of this project:**
**5.2 Scope:** This standard defines the e functional verification language.
This standard aims to serve as an authoritative source for the
definition of (a) syntax and semantics of e language constructs,
(b) the e language interaction with standard simulation languages
and (c) e language libraries.

**5.3 Is the completion of this standard dependent upon the completion of another standard:**
**5.4 Purpose:** This standard serves the community involved with functional
verification of electronic designs using the e language. It
provides an implementation independent definition of the e language
and facilitates the development of e language based design
automation tools.
**5.5 Need for the Project:** Due to the rapid evolution of verification technology, a number of new features have been introduced in IEEE 1647-2008 compliant products during the development of IEEE 1647-2010. This revision project will bring the standard up to date with respect to these features.
**5.6 Stakeholders for the Standard:** The stakeholders for the 'e' language are verification engineers for hardware, software and system projects and the tool developers for this community.

**Intellectual Property**
**6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?:** Yes
**If yes please explain:** The working group will solicit donations of manuals and possibly other copyrighted materials and will pursue appropriate copyright releases.

**6.1.b. Is the Sponsor aware of possible registration activity related to this project?:**

**7.1 Are there other standards or projects with a similar scope?:** Yes
**If Yes please explain:** Functional verification is addressed to some extent by the following projects: Verilog and SystemVerilog (1364 and 1800), VHDL (1076), System-C (1666), PSL (1850). SystemVerilog is listed below as the most relevant.
**and answer the following**   **Sponsor Organization:** IEEE Design Automation Standards Committee (DASC)
   **Project/Standard Number:** 1800
   **Project/Standard Date:** 09-Nov-2005
   **Project/Standard Title:** Standard for SystemVerilog: Unified Hardware Design, Specification and Verification Language
**7.2 Joint Development**
   **Is it the intent to develop this document jointly with another organization?:** No

**8.1 Additional Explanatory Notes (Item Number and Explanation):**