VHDL-AMS Survey and Call for Participation

The VHDL-AMS hardware description language is an extension of the VHDL language used since the late 1980s. Supporting the description and simulation of analog and mixed-signal devices, VHDL-AMS was first standardized as IEEE Std 1076.1 in 1999 and subsequently revised in 2007. VHDL-AMS is supported by tools from all the major EDA vendors as well as some of the smaller vendors, and it has been used in a variety of applications, mostly in IC and system design.

The IEEE P1076.1 Working Group is now starting with another revision of the language, and it is asking for your help. First, the WG has collected a number of possible language extensions, and it requests your input regarding the relative priority of these extensions. Second, the WG is looking for new members willing to participate in the work to define the language extensions. Participation in the work of the Working Group can take on many forms, including but not limited to:

- review and approval of requirements
- collection of detailed requirements
- definition of language extensions based on requirements
- review of language extensions
- creation of a new standard package
- testing of a new standard package

As you can see, the creation or extension of a standard requires many different skills. If you are interested in participating, please contact the WG Chair Ernst Christen, christen.1858@verizon.net. You can also find additional information about the IEEE P1076.1 Working Group at http://www.eda.org/vhdl-ams

An overview of the projects considered for the upcoming revision of VHDL-AMS can be found at http://www.eda.org/twiki/bin/view.cgi/P10761/ProjectsArea. There are three kinds of projects. **Upgrade Projects** and **Maintenance Projects** are mandatory for the revision as they are related to incorporating the changes in the base VHDL language and the 1076.1.1 companion standard into VHDL-AMS. The section **New Feature Projects** describes the projects for which we are requesting guidance. These projects have been proposed by users of VHDL-AMS over the past few years.

We would like you as a user of, or a person otherwise interested in, the VHDL-AMS language to give each New Feature Project a grade in the range 1 to 10 to reflect the importance this project has for you and your work, with 10 being the highest grade. We will then tally the responses, together with responses we received from the Working Group, to determine the priorities for these projects. The priorities may affect which projects will be included in the next revision of VHDL-AMS, depending on the number of people participating in the work to define these extensions. The New Feature Projects are:

..... Mixed netlists

..... Frequency domain modeling

..... Support for partial differential equations

..... Table-driven modeling

..... Vector/matrix operations

..... Unified use of SPICE models in different tools

Please grade each project according to the importance it has for you and your work. Enter the grade in the space provided. You are also welcome to submit at this time requests for additional new features to include in VHDL-AMS. We will consider such requests to the extent possible in the upcoming revision. Enter your suggestions in the space below.

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Return the completed questionnaire with your grades and suggestions to the Chair of the IEEE P1076.1 Working Group: Ernst Christen, christen.1858@verizon.net, by April 30, 2010.

Please also forward this email to other people that might be interested in either providing feedback to the WG or participating in the work to define the language extensions.

We are looking forward to your input and your help. If you have any questions please do not hesitate to contact me.

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