P1076.1

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Type of Project: Revision to IEEE Standard 1076.1-2007
PAR Request Date: 30-Dec-2010
PAR Approval Date: 31-Mar-2011
PAR Expiration Date: 31-Dec-2015
Status: PAR for a Revision to an existing IEEE Standard
Root Project: 1076.1-2007

1.1 Project Number: P1076.1
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard VHDL Analog and Mixed-Signal Extensions

3.1 Working Group: VHDL Analog and Mixed-Signal Extensions Working Group (C/DA/VHDL_AMS)
Contact Information for Working Group Chair
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3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)
Contact Information for Sponsor Chair
  Name: Stanley Krolikoski
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Contact Information for Standards Representative
  None

4.1 Type of Ballot: Individual
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 12/2012
4.3 Projected Completion Date for Submittal to RevCom: 10/2013

5.1 Approximate number of people expected to be actively involved in the development of this project: 12
5.2 Scope: This standard defines the IEEE 1076.1(TM) language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. Informally called VHDL-AMS, (VHSIC Hardware Description Language for Analog and Mixed-Signal, where VHSIC stands for Very High Speed Integrated Circuits), the language is built on the IEEE 1076(TM)(VHDL) language and extends it to provide capabilities of writing and simulating analog and mixed-signal models.

5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: To support the design and verification of complex electronic systems containing a mixture of analog and digital devices, the IEEE 1076.1(TM) language provides, as an extension of the IEEE VHDL 1076 language, a comprehensive set of capabilities for the description and simulation of mixed-signal and mixed-technology systems. The revision adds selected new features to the language definition of the 1076.1-2007 standard, and updates the 1076.1-2007

Old Scope: This standard defines the IEEE 1076.1 language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. The language, also informally known as VHDL-AMS, is built on the IEEE 1076(VHDL) language and extends it to provide capabilities of writing and simulating analog and mixed-signal models.

Old Purpose: To provide a comprehensive mixed-signal description and simulation capabilities as an extension to the IEEE VHDL 1076 language. The revision corrects editorial errors and clarifies aspects of the language definition in the 1076.1-1999 standard, and updates the 1076.1-1999
5.5 Need for the Project: Complex electronic systems comprise a mixture of digital and analog elements. This project defines a modeling language that allows engineers to use design automation tools to analyze and verify operation of designs prior to manufacture, thus improving productivity and avoiding the cost of erroneous designs. The language is of benefit to engineers and organizations developing mixed analog and digital systems for applications including consumer devices, telecommunications, control systems and automotive systems. Design automation tools based on the current standard are provided by a number of suppliers and are in use in industry.

5.6 Stakeholders for the Standard: The stakeholders are telecom, automotive, aerospace, Electronic Design Automation (EDA) vendors.

Intellectual Property
6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: Yes
If yes please explain: Since the 1076.1 standard is a superset of the 1076 standard, all copyrighted material included there is also part of 1076.1. In addition, two planned activities may depend on copyrighted material. This is currently under review.

6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

7.1 Are there other standards or projects with a similar scope?: Yes
If Yes please explain: Since IEEE Std 1076.1 was first approved in 1999, two standards with overlapping scope have become available:
Verilog-AMS 2.3.1, an Accellera standard, 6/1/2009
SystemC-AMS 1.0, an OSCI standard, 3/8/2010
Each of these standards provides analog and mixed-signal modeling capabilities within the syntactic and semantic framework of the corresponding digital language.

and answer the following
Sponsor Organization: Accellera Organization, Inc.
Project/Standard Number: Verilog-AMS 2.3.1, SystemC-AMS 1.0
Project/Standard Date:

7.2 Joint Development
Is it the intent to develop this document jointly with another organization?: No

8.1 Additional Explanatory Notes (Item Number and Explanation): 1. The revision incorporates changes in the base 1076 language introduced in its 2008 revision, adapts the 1076.1 definitions to be consistent with these changes, and adds selected new functionality to the language.
The revision of 1076.1 that is the topic of this PAR only focuses on the 2008 revision of 1076: it brings the enhancements made in 1076-2008 into the 1076.1 standard. That is, the 1076.1 revision is independent of the next revision of 1076, which by chance is about to start at the same time. Conversely, the planned 1076 revision is unaffected by this revision of 1076.1. There are individuals that participate in both efforts, so the two groups are aware of each others activities.