



## Working Group Meeting October 20, 2009

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WG Chair

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## Administrative Issues

- ◆ Approval of minutes of WG meeting on September 22
- ◆ Revision Ballot of IEEE Std 1076.1.1
  - Draft PAR approved by DASC on August 20
  - Draft PAR submitted to NesCom for October 23 meeting
  - Peter Ashenden offered to volunteer time to update the LRM
- ◆ Officer elections
  - Two year term of WG officers ends in December
  - Will select Returning Officer to run elections
- ◆ Review of IEEE patent policy
  - <http://standards.ieee.org/board/pat/pat-slideset.pdf>



## Agenda

- ◆ Call to order
- ◆ Approval of agenda
- ◆ Administrative issues
  - Minutes of last meeting
  - Revision of IEEE Std 1076.1.1: Current status
  - Officer elections
  - Review of IEEE patent policy
- ◆ Detailed review of new projects for revision of IEEE Std 1076.1
  - Partial differential equations
  - Table-driven modeling
  - Vector/matrix algebra
- ◆ Next meetings
- ◆ AOB
- ◆ Adjourn



## Table-driven Modeling: Introduction

- ◆ Definition
  - $f(x_1, \dots, x_n)$  described as a table of  $(n+1)$ -tuples
- ◆ Motivation
  - Pros
    - Users often have measured data that they want to use to create a model
    - Even if a device model exists, using a table model may yield faster simulations
  - Cons
    - Table models are only accurate in the range in which the function has been sampled
    - Using table models in a simulation may require large amounts of memory



## Table-driven Modeling: Requirements

- ◆ **Ability to describe  $(y_1, \dots, y_m) = f(x_1, \dots, x_n)$** 
  - As static data in a model
  - In a file read by an instance of the model
- ◆ **Ability to specify interpolation method between table points**
  - e.g. linear, quadratic, spline
- ◆ **Ability to specify behavior if a point  $(x_1, \dots, x_n)$  lies outside the table**
  - e.g. error, extrapolation, nearest value
- ◆ **Ability to specify tables whose grid is not fully populated**
- ◆ **Some degree of compatibility with Verilog-AMS**
- ◆ **More details (to be reviewed) at**  
[http://www.eda.org/vhdl-ams/old/ftp\\_files/extensions/TLU/requirements\\_tlu\\_modeling\\_in\\_vhdl-ams\\_2006-03.pdf](http://www.eda.org/vhdl-ams/old/ftp_files/extensions/TLU/requirements_tlu_modeling_in_vhdl-ams_2006-03.pdf)



## Table-driven Modeling: VHDL-AMS Thoughts

- ◆ **Create package to define necessary functionality**
- ◆ **Define overloaded functions to return an interpolated/extrapolated value**
  - Table data specified in file
  - Table data specified in the model
- ◆ **Define record types and one-dimensional array types of each**
  - e.g. type table2 is record x1,x2,y: real; end record;
- ◆ **Define record type to control interpolation/extrapolation, with elements of an enumeration type**
  - e.g. type dimctrl is record int: inttype; extlow, exthi: exttype; end record
  - Table function is called with an array of these
- ◆ **Should independent variables in function call be specified as an array or individually? This affects the number of overloaded functions needed.**
- ◆ **Is there a need for tables with integer x/y?**



## Table-driven Modeling: Verilog-AMS

- ◆ **\$table\_model(table\_inputs, table\_data, table\_control\_string)**
  - table\_inputs ::= expression { , expression }  $x_1, \dots, x_n$
  - table\_data ::= file\_name  
| array\_expression { , array\_expression } n+1 expressions
  - table\_control\_string ::= " [ dim\_seq { , dim\_seq } ] [ ; dep\_selector ] "
  - dim\_seq is a sequence of characters that specify interpolation method and extrapolation method at lower and upper end
  - dep\_selector is an integer that specifies a data column in the file
- ◆ **Table data in file is specified as rows of values**
  - Each row specifies values  $x_n, x_{n-1}, \dots, x_1, f_1(), f_2(), \dots, f_m()$
  - There may be additional values in each row that can be specified to be ignored in the table control string of a \$table\_model call
- ◆ **No ordering of table data required**
- ◆ **Interpolation/extrapolation is recursive and is always done in one dimension**



## Vector/Matrix Algebra: Introduction

- ◆ **Motivation**
  - VHDL-AMS supports quantities with scalar and composite types
  - Vector (1-dimensional array) types are often used to describe buses
  - The termination of a bus of length N can be expressed as
$$V = R * I$$
where V, I are N-vectors and R is a scalar
  - The behavior of an N-port transformer is expressed as:
$$V = d(L\_matrix * I) / dt$$
where V, I, flux are N-vectors, L\_matrix is a NxN-matrix
- ➔ **Vector/matrix algebra by means of overloaded operators possibly complemented by some additional functions**



## Vector/Matrix Algebra: Thoughts

- ◆ **Create package to define necessary overloaded operators:**
  - vector addition/subtraction
  - vector \* scalar, scalar \* vector, vector / scalar
  - inner vector product, outer vector product
  - vector \*\* scalar
  - matrix addition/subtraction
  - matrix product, matrix inversion
  - vector \* matrix, matrix \* vector
  - Probably others, e.g. element-wise vector product
- ◆ **Is there a need for these operators to be available?**
  - Nice to have is not good enough
- ◆ **Is there a need for these operators to be standardized?**
  - Users could write their own if needed



## Meeting Schedule

- ◆ **Meeting schedule once per month**
- ◆ **Web meetings most of the time**
- ◆ **Next meetings:**
  - Tuesday, November 17, 2009, 8am PST
  - Tuesday, December 15, 2009, 8am PST



## Projects not Reviewed

Project	Notes
Semantics for parameter sweeps	Requirement unclear, likely related to corner modeling
Unified C interface	Such an interface has been defined as part of VHPI
Support for HIL simulation	What are the requirements?
Standard symbol format	Symbol format standardized separately. Is there a need to define a VHDL-AMS standard attribute to link to the symbol file?
Specifications	White paper at <a href="http://www.eda.org/vhdl-ams/old/ftp_files/extensions/RV/RV_WP_0.2.txt">http://www.eda.org/vhdl-ams/old/ftp_files/extensions/RV/RV_WP_0.2.txt</a> gives introduction and then proposes syntax. What are the requirements?

