


IEEE DASC P1076.1 Working Group
<http://www.eda.org/vhdl-ams/>

**Working Group Meeting
July 8, 2015**

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Agenda

- ♦ **Call to order**
- ♦ **Approval of agenda**
- ♦ **Administrative issues**
 - Minutes of June 10, 2015 meeting
 - Review of IEEE patent policy
 - PAR status
 - Public reviews
- ♦ **Project discussions**
 - LCS 201x-03 Architecture statements: review follow-up
 - LCS 201x-04 Types and natures: review
 - LRM status
 - Table-driven modeling
- ♦ **Next meeting**
- ♦ **AOB**
- ♦ **Adjourn**




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Administrative Issues

- ♦ **Approval of minutes of WG meeting**
 - Meeting of June 10, 2015, available at <http://www.eda.org/vhdl-ams/>
- ♦ **Review of IEEE patent policy**
 - <http://standards.ieee.org/board/pat/pat-slideset.pdf>
- ♦ **PAR status**
 - Filed 2 year extension with IEEE
 - Supported by DASC
 - Responded to 3 questions/issues
 - 2 about size of Working Group
 - 1 about reason for delay (lost 1 year trying to find funding structure)
 - NesCom meeting on June 5 made recommendation to grant request
 - IEEE-SA Standards Board on June 11 approved PAR extension. The PAR is now valid till December 31, 2017




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Administrative Issues: Public Reviews

- ♦ **A standard is open for Public Review, in addition to the review given by participants in the ballot**
 - Informal in the past, with announcements in Trade press
- ♦ **Public Review process after July 6, 2015**
 - Projects about to be balloted are announced at <https://publicreview.standards.ieee.org>
 - Interested parties can purchase draft standard to give feedback
 - Public review starts concurrently with ballot
 - Ballot is open for 30 days
 - Public review is open for 60 days
 - All comments received from Public Review must be responded to
 - Public review material must be submitted to RevCom
- ♦ **Plan for 45 to 60 days of additional time from being ready to ballot till RevCom**



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LCS 201x-03 Architecture statements

♦ Two choices for organization of clause 11

- Hierarchical organization
 - Subsections for Concurrent statements and Simultaneous statements
 - Actual statements are moved one level down
 - Changes section numbering for all statements
 - Will create different section numbers in 1076 and 1076.1
- Flat organization
 - Simultaneous statements are added as new subsections
 - Concurrent statements retain their section number
 - Consistency between 1076 and 1076.1
 - Section numbers for Simultaneous statements will be stable unless new concurrent statements are added

♦ Statement classification

- Use traditional classification as concurrent and simultaneous stmts
- New classification: concurrent, structural, and simultaneous stmts



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LCS 201x-04 Types and natures

♦ Definitions to extend the changes to the type system regarding unbounded, fully constrained and partially constrained composite types to composite natures

- Array natures
- Record natures

♦ Changes mostly straightforward

♦ Clause 5 will need updates

- Predefined natures and array natures
 - To be done as part of 1076.1.1 integration
- References to other sections, in particular 6.11
 - To be done as part of updating the corresponding sections



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LRM Status

♦ We now have

- Individual files for clauses
 - Has conditional text enabled for everything
- An integrated document P1076.1-201x_D0.1.pdf containing all clauses
 - Has conditional text enabled for most tags, but not **VHDL only**

♦ Issue

- Some condition tags are wrong
 - **VHDL only** instead of **Added in 1076-2008**
 - Example: 1.3.4 Front matter
- Some text is unclear or misleading with **VHDL only** missing
 - Partial words, or missing parts of sentences
 - Example: 5.3.2.3 Predefined array types

♦ Recommendation: enable **VHDL only** in pdf to facilitate work



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Project Discussion: Table-Driven Modeling

♦ Resolution of open issues identified at last meeting

♦ Defaults for vector parameters of PREPARE_TABLE_DATA functions

- Is it possible to use something like


```
(..., dimension: integer, ...,
METHOD: INTERPOLATION_METHOD_VECTOR(1 TO dimension) := (others => TDM_PWL), ...)
```

 i.e. can a formal parameter of a subprogram appear in the declaration of another formal parameter?
 - This is not possible for the parameters of a subprogram, only for the generics of an entity
- Proposal:
 - Declare vector parameters long enough to handle all practical cases, use only the first *dimension* elements
 - Ensure that *dimension* does not exceed the length of the vectors
 - User will have to provide an actual argument for a vector only if
 - *dimension* > length of declared vector parameter
 - The default is not adequate for the table



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Project Discussion: Other



- ♦ **Vector/Matrix operations**
 - Status
- ♦ **Handling of copyrighted material**
 - No progress



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Project Planning – Reminder

- ♦ **Completion of projects:** **Q1 2016**
 - Based on current data
- ♦ **Completion of LRM and other documents:** **Q2 2016**
 - Packages, UML
- ♦ **First ballot:** **Q3 2016**
- ♦ **Second ballot:**  **Q2 2017**
- ♦ **RevCom:**  **Q3 2017**
- ♦ **Expiration of extended PAR:** **Q4 2017**
 - 2 year extension



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Next Steps

- ♦ **Handling of copyrighted material**
- ♦ **P&P revision**
- ♦ **Next meetings (announced at www.eda.org/vhdl-ams/):**
 - Wednesday, August 12, 2015, 8:00am PDT (15:00 UTC)
 - Wednesday, September 9, 2015, 8:00am PDT (15:00 UTC)



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