IEEE DASC P1076.1 Working Group

http://www.eda.org/vhdl-ams/

Working Group Meeting
January 12, 2010

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WG Chair

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Agenda

- **Call to order**
- **Approval of agenda**
- **Administrative issues**
  - Minutes of last meeting
  - Revision of IEEE Std 1076.1.1: Status
  - Officer elections
  - User survey
  - Status of reflector
  - Review of IEEE patent policy
- **Overview of VPI-AMS for Verilog-AMS**
- **Next meetings**
- **AOB**
- **Adjourn**

Administrative Issues

- **Approval of minutes of WG meeting held December 15, 2009**
- **Revision Ballot of IEEE Std 1076.1.1**
  - Draft PAR approved by DASC on August 20
  - Draft PAR submitted to NesCom for October 23 meeting
  - PAR approved by IEEE-SA on November 2, 2009
  - Peter Ashenden working on LRM, first draft by January 22
- **Officer elections**
  - Election results published January 5, 2010
  - All officers confirmed

Administrative Issues

- **User survey**
  - Ready to start, awaiting resolution of reflector problems
- **Status of reflector**
  - Since mid December messages from WG chair (as well as those of some others) are not being distributed to subscribers
    - Problem has been identified
  - Messages that were distributed were not recorded in email archive.
    - Caused by eager update of ownership of DASC files in response to election of new DASC chair. This has been fixed.
- **Review of IEEE patent policy**
  - http://standards.ieee.org/board/pat/pat-slideset.pdf

Overview of VPI-AMS for Verilog-AMS (1)

- **Extends VPI defined by IEEE Std 1364**
- **Overview is based on Verilog-AMS LRM V2.3.1**
- **Basic capabilities**
  - Access to information about elaborated design
  - Dynamic interaction with external application using callbacks
    - Simulation control
    - Definition/execution of user-defined system tasks and system functions
- **Based on abstract data model of design and simulation kernel**
- **VPI functions**
  - 7 new functions
  - Many existing functions extended to support analog needs

Overview of VPI-AMS for Verilog-AMS (2)

- **Access to information about elaborated design**
  - Extends the Verilog routines to traverse a design and to query information by also providing access to:
    - Disciplines
    - Natures
    - Conservative and signal-flow ports
    - Conservative and signal flow nodes
    - Branches
    - Flow and potential of a branch (called quantities)
    - Contribution statements

    and the data related to these items
  - It does not seem to be possible to create any of these

Overview of VPI-AMS for Verilog-AMS (3)

- **Dynamic interaction: Simulation interaction**
  - VPI functions to retrieve data
    - vpi_get_analog_value: value of flow or potential object
      - Real and imaginary part
    - vpi_get_analog_time: current simulation time
    - vpi_get_analog_delta: current time step
    - vpi_get_analog_frequency: current simulation frequency
    - vpi_get_real: simulation parameters
      - Start/end time
      - Maximum time step
      - Start/end frequency
  - Simulation control
    - Extends vpi_sim_control to support:
      - Request additional iterations
      - Reject a solution

Overview of VPI-AMS for Verilog-AMS (4)

- **Dynamic interactions: callbacks**
  - Register a function to be called for some reason, plus arguments the function is called with.
  - Callback reasons extended to include:
    - First analog solution
    - Last analog solution
    - Accepted analog solution at specified time
      - May force time point
    - Accepted analog solution at delta time
      - Forces time point
    - Convergence test
      - Allows rejection of solution and selection of earlier time
  - Remove callbacks
  - Get information about callbacks

Overview of VPI-AMS for Verilog-AMS (5)

- **Dynamic interactions: analog system tasks and functions**
  - Allows the definition and execution of foreign routines, which are called in the Verilog-AMS module like a predefined system task or system function
  - vpi_register_analog_systf: registers an analog system task of function
    - Extends vpi_register_systf and includes, among others:
      - Function to be called at compile time (e.g. to check arguments)
      - Function to return function value and optionally partial derivatives
      - Function to define how partial derivatives are computed and returned
  - vpi_get_analog_systf_info returns information about analog system tasks or functions
  - Partial derivatives
    - Elaboration time function defines what partials are computed
      - Can specify PD of function value or argument w.r.t. any argument
    - Simulation time function retrieves handle of a PD value to define using vpi_handle_multi, then returns value with vpi_put_value

Overview of VPI-AMS for Verilog-AMS (6)

- **Summary**
  - Supports purely analog models only
    - Mixed-signal behavior must be defined in Verilog-AMS model
  - Support for time domain simulation reasonably well defined
    - Functions are resistive
      - Reactive behavior must be defined in Verilog-AMS model
    - Functions must be cycle pure
    - Function values and partial derivatives are always computed together, which may have some overhead in certain cases
    - Some ambiguities and unclear definitions or examples
  - Support for small-signal frequency domain simulation unclear
    - Can retrieve frequency and quantity values, useful for logging
    - Definition of partials may allow small-signal model of an analog system task or function to be defined
    - No ability to specify small-signal stimulus
  - Support for noise simulation and other simulations not defined

Meeting Schedule

- **Meeting schedule once per month**
- **Web meetings most of the time**
- **Next meetings:**
  - Tuesday, February 9, 2010, 8am PST
  - Tuesday, March 9, 2010, at DATE, details TBD