P1076

Submitter Email: jim@synthworks.com
Type of Project: Revision to IEEE Standard 1076-2019
Project Request Type: Initiation / Revision
PAR Request Date: 12 Oct 2021
PAR Approval Date:
PAR Expiration Date:
PAR Status: Submitted
Root Project: 1076-2019

1.1 Project Number: P1076
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Project Title: Standard for VHDL Language Reference Manual
Change to Title: ~~IEEE~~ Standard for VHDL Language Reference Manual

3.1 Working Group: VHDL Analysis and Standardization Group(C/DA/P1076)
3.1.1 Contact Information for Working Group Chair:
Name: Jim Lewis
Email Address: jim@synthworks.com
3.1.2 Contact Information for Working Group Vice Chair:
Name: Patrick Lehmann
Email Address: patrick.lehmann@plc2.de
3.2 Society and Committee: IEEE Computer Society/Design Automation(C/DA)
3.2.1 Contact Information for Standards Committee Chair:
Name: Dennis Brophy
Email Address: dennis_brophy@mentor.com
3.2.2 Contact Information for Standards Committee Vice Chair:
None
3.2.3 Contact Information for Standards Representative:
None

4.1 Type of Ballot: Individual
4.2 Expected Date of submission of draft to the IEEE SA for Initial Standards Committee Ballot: Jun 2025
4.3 Projected Completion Date for Submittal to RevCom: Dec 2025

5.1 Approximate number of people expected to be actively involved in the development of this project: 30
5.2 Scope of proposed standard: This standard defines the syntax and semantics of the Verification and Hardware Description Language (VHDL). Historically the 'V' in the language's acronym came from the VHSIC (Very High Speed Integrated Circuits), which was the U.S. government program that funded the early work on the standard. Changing the 'V' to mean verification reflects the language's increasing usage for verification as well as design.
Change to scope of proposed standard: This standard defines the syntax and semantics of the ~~VHSIC~~ Verification and Hardware Description Language (VHDL). ~~The~~ Historically the 'V' in the language's acronym came from the VHSIC (Very High Speed Integrated Circuits), ~~in~~ which ~~the language's name comes from~~ was the U.S. government program that funded the early work on the standard. Changing the 'V' to mean verification reflects the language's increasing usage for verification as well as design.

5.3 Is the completion of this standard contingent upon the completion of another standard? No
5.4 Purpose: VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Since it is both machine and human readable, it supports the design, development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. This document is intended for the implementers of tools supporting the language and for advanced users of the language.
5.5 Need for the Project: General language enhancements to improve designer productivity and verification capability. In addition, it is desired to include the expired standard 1076.4 into 1076 as was done in 1076-2008 for 1076.2, 1076.3, and 1164.

Change to Need for the Project: General language enhancements to improve designer productivity ~~by allowing the specification of models more efficiently or the ability to specify functionality that was previously not possible or impractical to~~ and ~~specify~~ verification ~~in VHDL~~ capability . ~~Verification capabilities are needed to improve~~ In ~~the~~ addition, ~~quality of the~~ it ~~designs~~ is ~~and~~ desired to ~~address the significant and growing portion of~~ include the ~~electronic~~ expired ~~system~~ standard ~~design~~ 1076.4 ~~schedule~~ into ~~that~~ 1076 ~~is~~ as ~~being~~ was ~~spent~~ done in ~~ensuring the design is functionally~~ 1076-2008 ~~correct~~ for ~~before manufacturing~~ 1076 . ~~These capabilities directly address~~ 2, ~~productivity~~ 1076.3, and ~~quality~~ 1164 .

5.6 Stakeholders for the Standard: - IC and FPGA IP developers,
- IC and FPGA developers,
- IC and FPGA manufacturers,
- Embedded system developers,
- Embedded system manufacturers,
- Embedded system integrators,
- Electronics Design Automation (EDA) tool vendors

Change to Stakeholders for the Standard: -~~Digital~~ IC and FPGA IP developers , -~~Digital~~ IC and FPGA developers , - IC and FPGA manufacturers , -~~Digital~~ Embedded system developers, ~~and~~ - ~~embedded~~ Embedded system ~~developers~~ manufacturers , - ~~manufacturers~~ Embedded ~~and~~ system integrators,- Electronics Design Automation (EDA) tool vendors

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6.1 Intellectual Property

6.1.1 Is the Standards Committee aware of any copyright permissions needed for this project?
No

6.1.2 Is the Standards Committee aware of possible registration activity related to this project?
No

7.1 Are there other standards or projects with a similar scope? Yes

Explanation: There are three other projects with a similar scope: IEEE 1647 (e), IEEE 1800 (System Verilog), IEEE 1850 PSL
There is overlap between the capabilities of these languages. However, VHDL has been proven in the market and multiple commercial and open source tools currently support it.

Change to Explanation: There are three other projects with a similar scope: IEEE 1647 (e), IEEE 1800 (System Verilog), IEEE 1850 PSLThere is overlap between the capabilities of these languages~~/~~ . However, VHDL has been proven in the market and multiple commercial and open source tools currently support it.

~~cf. section 8.1 for additional details.~~

7.1.1 Standards Committee Organization: IEEE Design Automation Standards Committee (DASC)
Project/Standard Number: 1800
Project/Standard Date: 06 Dec 2017
Project/Standard Title: IEEE Standard for SystemVerilog-- Unified Hardware Design, Specification, and Verification Language

7.2 Is it the intent to develop this document jointly with another organization? No

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8.1 Additional Explanatory Notes: