

In 19.8, CHANGE:

For the first port, if neither a type nor a direction is specified, then it shall be assumed to be a member of a port list, and any port direction or type declarations must be declared after the port list. This is compatible with the Verilog-1995 syntax. If the first port type but no direction is specified, then the port direction shall default to **inout**. If the first port direction but no port kind or data type is specified, then the port shall default to a net of net type **wire**. This default net type can be changed using the `'default_nettype` compiler directive, as in Verilog.

TO:

For the first port, if neither a type nor a direction is specified, then it shall be assumed to be a member of a port list, and any port direction or type declarations must be declared after the port list. This is compatible with the Verilog-1995 syntax. If the first ~~port type~~ **port kind or data type is specified** but no direction is specified, then the port direction shall default to **inout**. If the first port direction **is specified** but no port kind or data type is specified, then the port shall default to a net of net type **wire**. This default net type can be changed using the `'default_nettype` compiler directive, as in Verilog.

In 19.8, CHANGE:

For an **inout** port, if the port kind is omitted, then the port shall default to a net of net type **wire**. This default net type can be changed using the `'default_nettype` compiler directive, as in Verilog.

```
// the inout port defaults to a net of net type wire
module mh2 (inout integer a);
...
endmodule
```

TO:

For ~~an inout port~~ **input and inout ports**, if the port kind is omitted, then the port shall default to a net of net type **wire**. This default net type can be changed using the `'default_nettype` compiler directive, as in Verilog.

```
// the inout port defaults to a net of net type wire
module mh2 (inout integer a);
...
endmodule
```

For output ports, if the port kind is omitted, the default port kind depends on how the data type is specified. If the port is declared without the `data_type` syntax, then the port kind defaults to a net of the default net type. This provides backward compatibility with Verilog. If the data type is declared with the `data_type` syntax, the port kind defaults to variable.

