

Proposal for ballot comment 156, Mantis item 505:

In 22.2, CHANGE:

A module, interface, program or class can have parameters, which are set during elaboration and are constant during simulation. They are defined with data types and default values. With System-Verilog, if no data type is supplied, parameters default to type `logic` of arbitrary size for Verilog compatibility and interoperability.

TO:

A module, interface, program or class can have parameters, which are set during elaboration and are constant during simulation. They are defined with data types and default values. ~~With System-Verilog, if no data type is supplied, parameters default to type `logic` of arbitrary size for Verilog compatibility and interoperability.~~ For compatibility with Verilog, if no data type is supplied, the type is determined when the value is determined.

and CHANGE:

In an assignment to, or override of, a parameter without an explicit type declaration, the type of the right-hand expression shall be unsized, real or integral.

TO:

In an assignment to, or override of, a parameter without an explicit type declaration, the type of the right-hand expression shall be ~~unsized~~, real or integral. If the expression is real, the parameter is real. If the expression is integral, the parameter is a `logic` vector of the same size with range `[size-1:0]`.