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## **Technical Committee Status** 04/14/11

Neil Korpusik  
P1800 Technical Chair

# SV-AC

- The following mantis items have been resolved

- 1756: The LRM doesn't indicate how control tasks \$asserton/off/kill affect verification statements in initial blocks
- 2386: Rename 16.9 to "Local variables"?
- 2412: Allow clock inference in sequences
- 2557: Rules for passing automatic variables to sequence subroutines are not clear
- 2839: Contradictory statement of increment/decrement operators usage.
- 3036: Explicitly allow unpacked data types for arguments of assertion system functions
- 3113: Add port\_identifier to constant\_primary BNF for sequences, properties and checkers
- 3135: Verbal explanation of nexttime and always is misleading for multiple clocks.
- 3376: triggered should be typeset as code

- Currently working on the following enhancements

- 2476: Need clarification about system functions \$onehot, etc
- 2804: Need to clarify rule (b) in 16.15.6 to allow inferred clock when expression appears in procedural assertion
- 3069: Relax rules for \$global\_clock resolution
- 3191: Allow sequence methods with sequence expressions
- 3295: need a way to control only asserts/covers/assume directives

- Status not updated from last time

# SV-BC

- Work in progress
  - Mantis 2388, 2856
    - Clarifying use of hierarchical references in constant expressions.
    - Children of mantis 3055 - "Design Construction Issues"
    - #4 priority for SV-BC
  - Mantis 210
    - "Generate for module port definitions"
    - #8 priority for SV-BC
- Email vote in-progress for 9 minor issues
  - Votes due by April 20, 2011

# Top-25 SV-BC Issues

Rank	Mantis ID	Summary
1	696	Parameterized tasks, functions
2	2310	Clarified Macro Semantics
3	3053	Virtual interface and interface-port issues
4	3055	Design construction issues
5	2991	Extension of enumerated types
6	1566	Variable number of task and function arguments
7	2114	Problems in definition of modports/abstract modports
8	210	Generate for module port definitions and instance port connections
9	3056	Master list of port issues
10	1084	Logical Expressions in Macros
11	2115	X-Optimism/X-Pessimism resolution
12	3073	Collected \$bits issues

Rank	Mantis ID	Summary
13	1697	Macro Loops
14	1202	define standard preprocessor
15	1251	x/z behavior in various contexts
16	2289	parameters inside comp unit and gen block are local
17	1504	Parameterized Structures (and Unions)
18	1144	Out-of-bounds array address
19	2081	always_comb statements
20	1553	nested module clarifications
21	2684	Variable part-selects
22	1861	Major enhancement of modports
23	1523	behavior of ?: on complex types
24	3074	Connectivity Enhancements
25	2124	`default_nettype var-type directive

# SV-CC

- Activity continues to be light
- Only addressing minor issues at this time
- Progress is being made on the top-10 issues
  - No proposals have made it to the SV-CC yet
- Concerned about ability to address many of them by the deadline
  - Will do a status update at Apr-27-2011 meeting

# SV-DC

- Met twice since the last Working Group meeting
  - Next meeting will be April 20<sup>th</sup>
- Mantis 3398
  - Discussing a joint proposal from Cadence/Mentor
  - User defined nets and resolution functions
  - Communicated details of proposal to Verilog-AMS committee
- New IEEE participation rules
  - Decreased attendance by ~25%
  - 3 Observers regularly attend
- Need to hold a new election of co-chair?
  - Jim Lear (Cirrus Logic) - co-chair

# SV-DC (cont)

- Requirements list for this PAR
  - Scalar real-valued nets
    - Real-valued nets with multiple drivers
    - Resolution functions for multiply driven real valued nets
    - Ability to represent X (unknown) and Z (undriven) states for real nets
    - Unidirectional and bidirectional ports with real nets
  - Aggregate nets with real-valued components
    - Constructs such as vectors, static arrays, structs and unions
    - Resolution functions for multiply driven aggregate nets
    - Unidirectional and bidirectional ports with aggregate nets
    - Atomic aggregate nets whose components resolved jointly (correlated resolution)
    - Ability to represent x, z states for atomic aggregate nets
  - Utilities for real-valued modeling
    - Definitions of math functions and relational operators for real types in the presence x and z states

# SV-EC SystemVerilog Testbench committee Update

## STATUS

- Held 3 regular bi-weekly meetings
- Mantis items review:
  - Reviewed proposal for mantis 3230 from sv-bc
    - SV-EC proposes to take ownership of 3230
    - Additional language in current LRM needs updating
  - Main Items from list of 25 being reviewed:
    - Mantis 2506 (Coverage)
    - Mantis 1356 (Multiple Inheritance)
    - Mantis 3278, 3279 & 2393 (related to 1356)
    - Mantis 3002 (AOP extensions)
  - A few simple mantis items were approved
    - Mantis 3181, 3297, 2952
    - Mantis 245 (close as already implemented)
    - Mantis 2985 (close as duplicate of 245)
    - Mantis 3405 (close as duplicate of 2952)

## Risks / Opens / Issues

- A few complex items on the review list may consume most of the available time.
- New P&Ps has affected user participation. Jonathan Bromley was very active.
- Doing both 1356 and 3002 could be difficult

## April/May 2011 PLANS

- Continue with high-level review.
- Finalize 1356, 2506, 3002 proposals for approval.
- Next regular meetings will be April 25, May 9th and May 16th 2011

# SV-EC Top-25 Mantis Items

top 25 Rank	Mantis ID	Number of Votes	weighted vote	Summary	Degrees of difficulty
1	2848	7	159	Is it legal to assign an interface containing class declaration to a virtual interface	med
2	3002	8	125	Aspect Oriented Programming (AOP) features	High
3	3046	8	112	Dotted names within inlined constraints	Low
4	1356	6	112	Multiple Inheritance	High
5	3001	9	102	Proper Polymorphic behavior of instantiation	low
6	2999	7	99	Class Handle reference inside of Constraints	med
7	3003	6	98	Constraint Composition	High
8	3082	7	96	(4) Ambiguity resolution (see slide 10 for examples of parts of the Standard that have been interpreted differently by different simulators)	
9	2845	4	84	virtual interface type checking versus interface type that had been defparam'ed	high
10	2956	4	76	clarify class 'process' definition (9.7 vs 18.13.3, 18.13.4, 18.13.5)	low
11	2505	4	76	class select: what is allowed after the dot?	low
12	2735	4	73	Ballot Comment #48: Chaining of method calls	med
13	1706	4	72	Meaning of static prefix for virtual interface assignments	
14	2488	4	69	Are virtual method calls legal within class constructors?	med
15	2112	6	69	Remove restrictions on NBA assignments to class members	med
16	3028	6	68	constraints for unique array elements.	Med
17	2950	4	67	virtual method prototype matching	low
18	2794	4	64	Clarify queue methods return status	low
19	2993	4	63	Cross cover points across different cover groups	med
20	1442	3	63	Clocking blocks legal in modports, missing from text description in 20.9	
21	2506 [2953]	6	61	Algorithmic generation of covergroup bin contents [2506 to replace 2953]	high
22	1349	5	61	fork/join none: what if parent thread terminates without blocking statement?	
23	2949	4	60	LRM is silent about the semantics of referencing a clocking block output	low
24	2451	6	58	Omitting body defaults	med
25	2987	6	56	Soft Constraints	med
	3278	Related to 1356		virtual method type rules	
	3279	Related to 1356		Enhance method override rules to allow covariant typing	
	3293	Related to 1356		Clarify \$cast behaviour on class handles	



# SV-FC

- No activity since the last Working Group meeting

# Champions

- Held an email vote for 19 mantis items
- Continuing the rate of 1 email vote per month
- Editor
  - Allowed to participate in Champions activities?