



ORACLE[®]



Technical Committee Status 10/14/10

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SV-AC

- The current focus is on checker usability enhancements
- The following mantis items have been resolved (no changes for some)

1678: Clarify that rewriting algorithm doesn't replace name resolution.

2095: Clarify meaning of distribution as condition for "disable iff"

2326: Rename 16.9 to "Local variables"?

2452: No vacuity information about synchronous aborts

2476: Need clarification about system functions \$onehot, etc

2494: 37.44 Assertion diagram missing restrict

2551: trivial example error

2558: Restriction inside checker construct

2571: confusing assertion clock inference rule

2732: Clarify timing diagram in Figure 16-4. Future value change

2754: Can clock change in conditional branch of 'if' operator

2804: Need to clarify rule (b) in 16.15.6 to allow inferred clock when expression appears in procedural assertion

3008: In \$past BNF, "expression" should be "expression1"

3134: sequence and property range parameters are erroneously defined

- **The committee would like to get permission to work on**

3206: Deferred assertions sensitive to glitches

3191: Allow sequence methods with sequence expressions

3195: Local Variables Flow Out Issue in and/or/intersect/implies

SV-BC October Update

- ▶ Close to resolving 1 issue so far: Mantis 696

- ▶ From the September 27, 2010 Meeting:

The SV-BC cannot build momentum behind a vision to significantly improve interfaces and related features while maintaining backward compatibility with the current definition.

How to significantly improve or redesign interfaces is not clear and the SV-BC is not making progress to address the situation.

- ▶ The SV-BC will pursue resolution of point issues.
- ▶ The SV-BC requests that the I800 WGG consider the scope of improving interfaces and facilitate a long-term, cross-committee effort to improve interfaces in future standards.

Top-25 SV-BC Issues

Rank	Mantis ID	Summary
1	696	Parameterized tasks, functions
2	2310	Clarified Macro Semantics
3	3053	Virtual interface and interface-port issues
4	3055	Design construction issues
5	2991	Extension of enumerated types
6	1566	Variable number of task and function arguments
7	2114	Problems in definition of modports/abstract modports
8	210	Generate for module port definitions and instance port connections
9	3056	Master list of port issues
10	1084	Logical Expressions in Macros
11	2115	X-Optimism/X-Pessimism resolution
12	3073	Collected \$bits issues

Rank	Mantis ID	Summary
13	1697	Macro Loops
14	1202	define standard preprocessor
15	1251	x/z behavior in various contexts
16	2289	parameters inside comp unit and gen block are local
17	1504	Parameterized Structures (and Unions)
18	1144	Out-of-bounds array address
19	2081	always_comb statements
20	1553	nested module clarifications
21	2684	Variable part-selects
22	1861	Major enhancement of modports
23	1523	behavior of ?: on complex types
24	3074	Connectivity Enhancements
25	2124	`default_nettype var-type directive

SV-CC

- Has been meeting regularly (every 2 weeks)
- There are a few Mantis Items with proposals
 - Are being reviewed
 - None of them have made it out of the SV-CC yet

SV-DC

- Approved a roadmap on 2010-09-15
 - This was sent as a separate pdf file
- Executive Summary:

The SV-DC intends to provide capabilities in SystemVerilog to support efficient modeling of analog/mixed-signal circuit components. These models are to be simulated by the event-driven simulation engine and should, therefore, exhibit simulation performance comparable to digital models and be suitable for system level simulation. The new modeling capabilities will be achieved by natural extensions to the existing SystemVerilog language; no analog solvers or netlist manipulations will be required.

SV-DC (cont)

- Summary of MUST requirements:
 - Scalar real valued nets
 - Aggregate nets with real valued components
 - Resolution functions for multiply driven nets of the above net types
 - Ability to represent X (unknown) and Z (undriven/high impedance) states for the above net types
 - Atomic aggregate nets whose components are resolved jointly (correlated resolution)
- **SV-DC requests permission to begin work on MUST and SHOULD roadmap items**

SV-EC SystemVerilog Testbench committee Updates October 14 2010

[last update August 10 2010]

STATUS

- Regular bi-weekly meetings
- Participation has been consistent
- From the 25 items:
 - 7 mantis item proposals have been approved: 2596, 3028, 2950, 2794, 1349, 2949, 2451
 - 8 mantis items were voted to be closed by email vote on Aug 28 2010. 251, 802, 1672, 1740, 2018, 2022, 2080
 - Mantis 2953 [algorithmic generation of covergroup bin contents] **a request is being made to p1800: allow sv-ec to review 2506 as a super-set of 2953.** [2953 had ranking 21, 2506 ranking of 39 during sv-ec voting for top 25]

Risks / Opens / Issues

- The new voting policy may hamper effective participation from previous usual attendees.
- A few complex items on the review list may consume all available time.

October-December 2010 PLANS

- Continue with high-level review.
- Review champions' comments on closed and approved mantis items.
- Review more proposals for approval.
- Next meeting Oct 25, Nov 8, 22, Dec 6th.

SV-EC top 25

top 25 Rank	Mantis ID	Number of Votes	weighted vote	Summary	Degrees of difficulty
1	2848	7	159	Is it legal to assign an interface containing class declaration to a virtual interface	med
2	3002	8	125	Aspect Oriented Programming (AOP) features	High
3	3046	8	112	Dotted names within inlined constraints	Low
4	1356	6	112	Multiple Inheritance	High
5	3001	9	102	Proper Polymorphic behavior of instantiation	low
6	2999	7	99	Class Handle reference inside of Constraints	med
7	3003	6	98	Constraint Composition	High
8	3082	7	96	(4) Ambiguity resolution (see slide 10 for examples of parts of the Standard that have been interpreted differently by different simulators)	
9	2845	4	84	virtual interface type checking versus interface type that had been defparam'ed	high
10	2956	4	76	clarify class 'process' definition (9.7 vs 18.13.3, 18.13.4, 18.13.5)	low
11	2505	4	76	class select: what is allowed after the dot?	low
12	2735	4	73	Ballot Comment #48: Chaining of method calls	med
13	1706	4	72	Meaning of static prefix for virtual interface assignments	
14	2488	4	69	Are virtual method calls legal within class constructors?	med
15	2112	6	69	Remove restrictions on NBA assignments to class members	med
16	3028	6	68	constraints for unique array elements.	Med
17	2950	4	67	virtual method prototype matching	low
18	2794	4	64	Clarify queue methods return status	low
19	2993	4	63	Cross cover points across different cover groups	med
20	1442	3	63	Clocking blocks legal in modports, missing from text description in 20.9	
21	2953	6	61	Algorithmic generation of covergroup bin contents	high
22	1349	5	61	fork/join none: what if parent thread terminates without blocking statement?	
23	2949	4	60	LRM is silent about the semantics of referencing a clocking block output	low
24	2451	6	58	Omitting body defaults	med
25	2987	6	56	Soft Constraints	med

SV-FC

- Not active
- Not expected to be needed for this PAR

Champions

- Conducted an email vote on the first 40 resolved mantis items
 - Feedback was sent back to the TC's for 9 items
 - 6 were sent back for changes
 - 2 friendly amendments
 - 1 was in the form of a question, which has been answered
- There are about 36 more in the resolved state
 - All 38 will be put up for an email vote
- Expecting Champions to be “caught up” by next WG meeting