March 18, 2005

Dear Colleague:

Following are the logistics and agenda of our next SystemVerilog work group F2F meeting.

Date:

Tuesday, April 19 2005, 09:00 am – 5:00 pm US Central Time (GMT -06:00)

The meeting will be held at:

IBM Austin, Building 906, Conference Room 2G-005
11501 Burnet Road,
Austin, 78758, Texas

For your convenience, I have attached the following links:

1. A map of directions from Austin Bergstrom Airport to IBM
2. A map of the IBM Site at Austin, so you can easily locate building 906
3. A list of Hotels that are close to IBM and are in the IBM recommended hotels list
4. A good site that may help you find more information on Austin and hotels would be: http://austin.citysearch.com/. The Arboretum area is nice and not far from IBM. There is a bunch of hotels there.

Dial-In Instructions:

Dial-In direction will be sent by Dennis Brophy

Dennis Brophy will also setup a **WebEx** invitation to the group, in order to enable follow-up on any presentations being done at the meeting by those who cannot attend in person. Registration information will be sent along the same note.

The chair of the meeting is:

Johny Srouji
IBM Corporation
Austin, 78758, TEXAS
United States
tel: 512 – 838-0252
fax: 512 – 838-2132
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Agenda

1) Call to order - Introductions & Affiliations
2) Approve agenda
3) Call for Patents
4) Approval of 17 February 2005 meeting minutes
5) Action Items Review and Follow-up
    a. A modified actions list is attached
6) Status Update on members fees collection – Dennis Brophy
7) P1800 Financial report update – Victor Berman / Oz Levia / Noelle Humenick
8) Ballot Status Update for SystemVerilog and Verilog – Johny Srouji / Noelle Humenick
    a. A list of voting entities and their voting status
    b. Summary of received issues and categorization
9) Detailed status update on SystemVerilog ballot issues resolution as were processed by the Champions and Technical Committees – Karen Pieper
    a. Discussion, Voting and Ratification of these issues – by P1800 voting WG members
10) Detailed status update on Verilog ballot issues resolution as were processed by the Champions and Technical Committees – Tom Fitzpatrick / Neil Korpusik
    a. Discussion, Voting and Ratification of these issues – by P1800 voting WG members
11) Incorporation of approved ballot issues to SystemVerilog and Verilog Drafts – Stu Sutherland
12) Discussion and decision on technical committees work and operation – Johny Srouji
    a. Short term: during the ballot review processes
    b. Mid term: until SystemVerilog and Verilog-2005 are approved by IEEE
    c. Long term: after the IEEE approval
13) Review, Modification & Tracking of P1800 WG schedule – Johny Srouji / Noelle Humenick
    a. Solidify detailed plans, issues and actions for P1800 LRM draft readiness for RevCom
14) New business
15) Next meeting (announce date, time, and location, if known)
16) Adjournment

Sincerely,

Johny Srouji, IBM, P1800 Work Group Chair