

SystemVerilog P1800 PAR input collection

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Synopsys Position on P1800 PAR

- SystemVerilog is very important to Synopsys as both Producer and Consumer of the standard.
- Synopsys supports continued evolution of SystemVerilog standard.
- Addressing Errata and Clarification is necessary for improved quality of SV
- User-guided enhancements are necessary to keep evolution of the standard in sync with needs of the user demand.

Proposed Approach

- Collect suggestions prior to writing PAR
 - Write PAR, keep the scope flexible
 - Prioritize suggestions (incl Mantis items)
 - Estimate efforts and champions
 - Draw a line ...
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- User-guided enhancements will keep the WG vibrant.
 - Many outside factors will influence user requests. Please do not make PAR so narrowly focused that good ideas will be tabled for 3+ years.

Thank You