RF/Analog Functional Modeling

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Background

• Qualcomm has focused effort on functional verification for all of RF/Analog products and cores. One key to this effort is to be able to model RF/analog circuits using an event based simulator.

• Methodology has evolved over the past 5 years and for the past ~3 years, we have settled on a common methodology for all projects. This methodology utilizes a Verilog PLI to enable this modeling.

• The PLI methodology has been in wide used in production for more than 3 years on at least 20-30 products

• Qualcomm would like to introduce similar concept to System Verilog and phase out the use of the current PLI solution.

Why System Verilog?

• Event based simulation enables large capacity including integration for large scale SOC's. Designs continue to get more complex and there exists even a greater need to functionally simulate the boundaries between Analog and Digital.

• Natural progression to cover RF/Analog functional rather than going into the SPICE/continuous time domain (AMS).

-Verilog A/AMS does not provide needed capacity/performance

-Focus is on functionality and not electrical performance

• Leverage System Verilog for improved verification capability regarding the RF/Analog interface to digital.

Proposal

• Support placing any defined standard type (logic, integer, real, string) or compound type (array, structure, union) on a single port or wire, and define custom resolution / interface functions to connect same or different types.

-The wire in the schematic / netlist defines connectivity only

-Simulator interprets net types and inserts appropriate resolution or interface function

For example an RF signal would look like:

[0.10, 0.12, 2e9, 10e6, 0.25]

[I, Q, fc, bw, vdc]

• Propose standard resolution functions for the “analog wire structure” to coverage voltage, currents or arbitrary real data types

• Able to define custom resolution functions for custom data types that are used

Next Steps…

- Appears to be significant interest across the industry – feedback from each major EDA vendor.

- Where does this belong? Accellera or IEEE?

Reference

- Chen, J.E.; , "A modeling methodology for verifying functionality of a wireless chip," *Behavioral Modeling and Simulation Workshop, 2009. BMAS 2009. IEEE* , vol., no., pp.96-101, 17-18 Sept. 2009
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