P1800 input from SV-BC

26/Feb/2010

SV-BC membership

The **Basic/Design Committee (SV-BC)** was responsible for the specification of the design features of SystemVerilog.

Matt Maidment, Intel Corporation, *Chair*
Brad Pierce, Synopsys, Inc., *Co-Chair*

Tom Alsop, Intel Corporation
Shalom Bresticker, Intel Corporation
Heath Chambers, HMC Design Verification, Inc.
Cliff Cummings, Sunburst Design, Inc.
Alex Gran, Mentor Graphics Corporation
Mark Hartoog, Synopsys, Inc.
Francoise Martinolle, Cadence Design Systems, Inc.
Don Mills, LCDM Engineering
Karen Pieper, Accellera, Tabula, Inc.
Dave Rich, Mentor Graphics Corporation
Steven Sharp, Cadence Design Systems, Inc.
Stuart Sutherland, Sutherland HDL, Inc.
Gordon Vreugdenhil, Mentor Graphics Corporation
Doug Warmke, Mentor Graphics Corporation

Methodology

- All subscribers of the SV-BC email reflector were asked to submit their #1 enhancement request and a justification.
- Their responses were consolidated on a web page: What is SV-BC saying?

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- Little appetite for enhancements.
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Specific trouble spots

- Macro preprocessor
- Separate compilation
- Raising the abstraction level of functions, as with parameterization or templates
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