IEEE P1800 SystemVerilog Working Group
Open Requirements Gathering Meeting
26 February 2010
8:00 a.m. – 10:00 a.m. PST
San Jose, CA USA

1 CALL TO ORDER - INTRODUCTIONS & AFFILIATIONS

The meeting was called to order at 8:05 a.m. PST.

Registered Participants:

Name	Affiliation
David Gates	AMD
Daniel Schostak	ARM
Rishiyur Nikhil	Bluespec, Inc.
Charles Dawson	Cadence
Chuck Berking	Cadence
Scott Cranston	Cadence
Stan Krolikoski	Cadence
Stefen Boyd	Cadence
Tsuneyoshi Yakabe	Cadence
Hseuh-Lin Kung	Cisco
Tony Tsai	Cisco
Jonathan Bromley	Doulos
Kaiming Ho	Fraunhofer
Hillel Miller	Freescale
John Havlicek	Freescale
Rozenberg Idan	Freescale
Sri Chandra	Freescale
Erik Seligman	Intel
Irina Lavva	Intel
Matt Maidment	Intel
Thanapoom Lertpanyavit	Intel
Alex Gran	Mentor Graphics
Bakalar, Kenneth	Mentor Graphics
Dave Rich	Mentor Graphics
Dennis Brophy	Mentor Graphics
Doug Warmke	Mentor Graphics
Gordon Vreugdenhil	Mentor Graphics
John Shields	Mentor Graphics
Ray Ryan	Mentor Graphics
Anders Nordstrom	OneSpin Solutions
David, Jonathan	Qualcomm
Jim Caravella	Qualcomm

Gary Delp	Self
Heath Chambers	Self
John Michael Williams	Self
Kevin Cameron	Self
Peter Flake	Self
Neil Korpusik	Sun
Thomas Thatcher	Sun
Cliff Cummings	Sunburst Design
Arturo Salz	Synopsys
Brad Pierce	Synopsys
Dave Cronauer	Synopsys
Greg Jaxon	Synopsys
Eduard Cerny	Synopsys
David Scott	Synopsys
Mark Hartoog	Synopsys
Mehdi Mohtashemi	Synopsys
Surrendra Dudani	Synopsys
Yatin Trivedi	Synopsys
Karen Pieper	Tabula
Michiel Ligthart	Verific
Scott Roland	Verilab
Bryan Ramirez	Xilinx
Premduth Vidyanandan	Xilinx
Stacey Secatch	Xilinx

2 PRESENTATIONS ON REQUIREMENTS FOR NEXT REVISION

Presentations were given by the following:

- Gary Delp, representing 1801 and 1685 presented.
- Mehdi Mohtashemi, representing 1800 SV-EC presented.
- Charles Dawson, representing 1800 SV-CC and Cadence Design Systems presented.
- Tom Thatcher, representing 1800 SV-AC presented.
- Brad Pierce, representing 1800 SV-BC presented.
- John Shields, representing 1735 presented.
- Ken Bakalar, representing Verilog-AMS presented. (Presentation shared at meeting was not submitted for meeting archive.)
- Jonathan David, representing Qualcomm presented.
- Cliff Cummings, representing Sunburst Design presented.
- John Havlicek, representing Freescale presented.
- Matt Maidment, representing Intel presented.
- Peter Flake, representing ELDA presented.
- Jonathan Bromley, representing Verilab presented.

- Geoff Barnes, representing Thales was presented by Brad Pierce
- Daniel Schostak, representing ARM presented.
- Dave Rich, representing Mentor Graphics presented.
- Yatin Trivedi, representing Synopsys presented.
- Neil Korpusik, representing Sun presented.
- Rishiyur Nikhil, representing Bluespec presented.
- Anders Nordstrom, representing One Spin presented.
- Tony Tsai, representing Cisco presented.

A single PDF with all the presentations merged, can be found here.

3 DISCUSSION

The group then discussed the items and issues that surfaced from the presentations. A discussion on a two-year or four-year timeline for the next standard did not end with a conclusion. A list was generated and each attendee was offered 8 points to give to the listed items. Users and Producers were totaled separately. The list resulted in the following list, ranked by Producer ordinals. The top 5 ordinals for Producers and Users are in bold.

Item	User	Producer	Combined	User Ordinal	Producer Ordinal	Combined Ordinal
Cleanup and Ambiguity Resolution -Rationalize the type system	31	56	87	**1**	**1**	**1**
AOP	25	5	30	**2**	8	**2**
Design Connectivity features (Cliff's X's)	16	1	17	**3**	17	5
Assertions & Checkers - The letter "t" - Real value assertions	15	6	21	4	7	4
Ease of use - Macros - Executable includes - Generates	13	2	15	5	14	8
Covergroups	10	3	13	6	11	10
Multiple Inheritance	8	3	11	7	12	11
Parameterized functions; variable number of arguments	6	4	10	8	9	12
Deprecating Features	6	4	10	9	10	13
Constraint Improvements	5	0	5	10		16

Connections to Analog -Verilog AMS -RF	4	17	21	11	**2**	**3**
Interfaces	3	12	15	12	4	7
General Directions & Vision	2	14	16	13	**3**	6
IEEE 1735/Encryption	2	3	5	14	13	
VPI/DPI Interactions	2	2	4	15	15	17
BlueSpec SV Enhancements	2	11	13	16	5	9
VCD	1	2	3	17	16	18
Class-based interface	1	7	8	18	6	14
Links to SystemC 1p (1p)	0	1	1	19	17	19
"DOT" Standards	0	0	0	20	20	20
Top-Down goals to drive lower groups (Vision)	0	0	0	21	21	21

The Excel spreadsheet for the information above can be found here.

4 MEETING CONCLUSION

The meeting concluded at 4:30 p.m. PST.