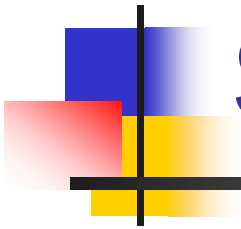
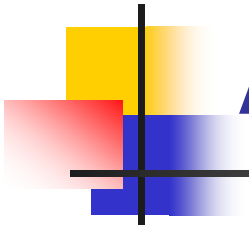


SV-XC committee

Somdipta Basu Roy (TI)
Loganath Ramachandran(Synopsys)

Feb 20, 2007



Activities

- Held 5 meetings
  - Alternate Wed 8-10 (PST)
- Very active participation
  - TI, Freescale, ADI, Sonics (6)
  - Cadence, Mentor , Synopsys (14)
- Website is now available
  - http://www.eda.org/sv-xc
- Hypermail archives in operation

Team Focus

- Interoperability of SystemVerilog with
  - SystemC, VHDL, VerilogAMS
- Most discussion focused on prioritization as the scope is broad
- Some of the issues are common across all the languages
  - Team will first work on common framework encompassing inter-operabilty in general
    - Scheduling semantics, Network resolution, name mapping
    - Paremter/generics, Binding, API
  - Smaller teams to work on specific language combinations
- Detailed questionnaire completed
  - http://www.eda.org/sv-xc/otherdocs/survey1.0.txt
  - Helps to identify the set of issues that we need to tackle
  - Will seek inputs from user community

Concerns/Issues

- Scope quite broad
  - Keeping discussions focussed on team charter is important
- Common framework issues will take more than a year
- Need to finalize intersection points with 2008 LRM schedules
- Some committee members interested in a dot standard (too early to decide?)
- Partnership with other language committees need to be established for better alignment with their efforts
- Increase participation from users/vendors