

P1800 & P1364

STATUS

- Technical committees are working on Errata and Enhancements
 - Resolutions for 169 issues approved by the WG
- New PAR version has been granted
- Technical Editor bid and selection in process
 - Decision expected in 11/9 WG meeting
- SystemVerilog full day tutorial for DAC was delivered
 - 100 persons attended
 - Presentation was well received
- New officers appointed
 - Karen Pieper, Chair
 - Neil Korpusik, Vice Chair
 - Dennis Brophy, Secretary

Risks / Opens / Issues

- Merge of 1364 into SystemVerilog given the number of issues already passed

H2'06 PLANS

- Target a two years revision of the language
- Merge with 1364; SVA enhancements; “local” enhancements; Errata; Integration to AMS; VHDL; SystemC; and other languages

IEEE 1800 – SV-AC

STATUS

- About 12 active members in SV-AC
- Working on Errata and Enhancements
 - As of today, 35 items logged on Mantis for SV-AC
 - Resolved: 6
 - Assigned: 14
 - New non-assigned: 15
- Item 1530 is a set of ppt presentations on potential enhancements
- Committee met every week on the last 2 months
 - ½ time spent on presentations by Dmitry on enhancements (item 1530)
 - ½ time spent on errata
- Several require involvement of the other committees
 - Argument types and qualifiers for properties and sequences
 - Generate in properties and sequences
 - Type query functions
 - Generalized use of error reporting functions

Risks / Opens / Issues

- Stabilization of existing functionality (errata) vs. enhancements (e.g., 1530)
- Focus on resolving issues

Q4'06 PLANS

- Prioritize errata and enhancements (under way)
- Process high priority errata to reach resolution
- Engage with other committees on enhancements that reach outside assertions

SV-EC SystemVerilog Testbench committee

STATUS

- Biweekly meetings re-started from December 2005
 - Approved 47 mantis items
 - Closed 7 mantis items
- Many additions to sv-ec reflector
 - Indicates higher levels of interest in technical issues being discussed and reviewed in the committee
- SV-EC face-to-face held on Nov 6th 2006
 - Main discussion on clocking-block, program-block and scheduling semantics.

Risks / Opens / Issues

- Many mantis/errata items have no proposals yet

Q4'06 PLANS

- Continue with review of mantis items containing proposals
- Plan on assigning the remaining mantis items to individual contributors for review and closure

November 8th 2006

V-AMS Proposal

- The Verilog AMS committee would like to become a part of SV
 - Would keep the languages closer in sync
 - Would significantly expand the SV-LRM (additional 400 pages)
- Recommended path
 - V-AMS as a “dot” standard of P1800
 - V-AMS representation on SV-XC

Scope for the SV-XC

- The SV-XC is responsible for defining the interface between Verilog 2008 and external hardware description languages such as: VHDL, V-AMS, SystemC.
 - In particular, simulation cycle coordination, how do types match, naming conventions, VPI/API, definition of network semantics, simulation initialization, and so on.
 - They are responsible for coordinating their work with equivalent efforts on the part of the other languages to ensure that the system of languages agree on both sides of the interface.
- This committee will report into the Technical Chair of the P1800, and will have representation on the Champions.
- Somdipta Basu Roy of TI has volunteered to Chair
- Logie Ramachandran has volunteered to Co-Chair