

P1800 2006 Direction

- **Must**

- Drive SystemVerilog market acceptance
- Productize SystemVerilog
 - Handle Errata
 - Add support for missing features
- Develop practical SVA language and methodology
 - Establish standard SVA library that can be used in context
 - Get the power of PSL into SVA
 - etc.

- **High**

- Review Verilog 1364 specify, timing checks and UDP
- Merge AMS and SystemVerilog

- **Nice to have**

- Merge Verilog 1364 and SystemVerilog
- VHDL and SystemVerilog interoperability