

# IEEE P1800 Structure Proposal

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SystemVerilog

# Agreed Upon

- IEEE SystemVerilog standard publication by October 2005
- P1800 Objectives:
  - Short Term: Standardize Accellera SV3.1a under IEEE while meeting our schedule
    - Cleanup, Clarification and Errata
  - Long Term: Alignment between Verilog 1364 and P1800 SystemVerilog into one RTL language
    - Potential enhancements to resolve inconsistencies between the two languages

# Errata Technical Committee

- Adopted Accellera four technical committees to form a P1800 sv- $\{ac, bc, cc, ec\}$  to work on resolving Errata
- Errata work group, chaired by Karen Pieper, own P1800 technical committees and report into P1800 WG
  - Charter: Collect, Prioritize and Resolve Errata issues
  - Issues are ratified by P1800
- Rules and Processes for Errata WG operation were defined, reviewed and ratified

# Champions

- A group of Verilog and SystemVerilog experts who are chartered to:
  - Oversee language modifications and maintain consistency within different aspects (design, assertions, test bench, etc)
  - Review all approved proposals by technical committees before they are presented for ratification by P1800
  - Alert potential inconsistencies with Verilog
- Group was identified – chaired by Karen Pieper

# Verilog 1364 Committees

- Proposal:
  - Maintain the operation of 1364 ETF to focus on Verilog Errata and their resolution
    - Should report to P1800
    - Operate under same P&P as defined for SV Errata
  - Merge 1364 PTF and P1800 sv-cc into one group
  - 1364 BTF – to be determined after Victor Berman report out

Appointed Chair: *Johny Srouji*

## IEEE P1800 SystemVerilog WG

Vice chair - TBD

Secretary: Dennis Brophy

Program Mgr: Noelle Humenick

LRM - TBD

Errata Chair: *Karen Pieper*

## P1800 Errata WG

Champions

## 1364 Verilog

SV-  
BC

SV-  
EC

SV-  
AC

SV-CC &  
PTF

BTF

Encryption

Errata

(transfer/merge)