



SystemVerilog



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Summary Of Errata – August 9

General Status

- Total Number of Errata is 153. (Reporters are: Synopsys, Cadence, JEITA, Mentor, Freescale, Infineon, Novas, Intel).
- More than 90% are clarification, typo and few are BNF errors or inconsistencies.
- We carried few enhancements since SystemVerilog 3.0.
 - We do not plan to address any enhancement.
- We prioritized the entire list (low, medium and high). The 90% is of high priority.
- They can be all resolved and edited in the LRM within one week.

Process: Errata Resolution

- Developers (10) will provide proposals.
 - Also an Errata Reporter can provide a proposal at the same time of entering errata.
- A group of experts will discuss and vote (IEEE voting).
 - Errata Subgroup understand that final decision maker is SystemVerilog WG.
 - Once accepted, the item is closed.
- LRM editor should examine the svdb and copy each resolution into the LRM.

Plans for moving Forward

- Increased Number of Developers From 6 to 10.
- Define a complete process for address errata.
 - This include Errata classification, prioritization, resolution, recommendation and acceptance.
 - New chair should write this up and committee should approve.
- We suggest a deadline for errata reporting in order for them to be processed. This will help to set milestones :
 - Errata resolution.
 - Final LRM Draft to be submitted to WG.



LRM Language

- Assign the LRM editor to modify the language based on an agreed style.
 - Assign couple of people to review the language modification to ensure no loss of information.
 - This should not take more than a week.
- In my opinion the LRM as is, is in a good style.

SV-3.1A -- Errata Status

By Status	Open	Resolved	Closed	Total
new	68	0	0	68
confirmed	1	0	0	1
assigned	60	0	0	60
resolved	0	23	0	23
closed	0	0	1	1



Errata Status -- Committee

By Category	Open	Resolved	Closed	Total
SV-AC	4	0	0	4
SV-BC	69	12	0	81
SV-CC	37	1	0	38
SV-EC	19	10	1	30



Errata Reporter - Status

Reporter Stats	Open	Resolved	Closed	Total
Pieper + JEITA	43	17	0	60
bpierce	32	0	0	32
sv-cadence	28	0	0	28
sv-mentor	11	0	0	11
daver	8	0	0	8
dwsmith	1	5	1	7
sv-novas	5	0	0	5
mittra	0	1	0	1
sv-freescale	1	0	0	1

Errata Developers - Status

Developer Stats	Open	Resolved	Closed	Total
salz	0	11	0	11
joao	27	1	0	28
daver	8	1	0	9
dudani	1	0	0	1
bpierce	23	0	0	23
Ray_Ryan	1	2	0	3

