

P1800 SystemVerilog

Proposed Operation Guidelines & Structure

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Presentation Objectives

- P1800 SystemVerilog WG Objectives
- Technical committees operation (transferred from Accellera)
- 1364 technical groups scope and operation under P1800
 - Pending modified PAR approval

P1800 Objectives – short term

- Standardize Accellera SV3.1a through IEEE standards and processes with highest efficiency
 - Goal: IEEE SV LRM DRAFT by DAC 2005 and approved standard by end of 2005
 - Process will include Cleanup, Clarification and Errata of SV3.1a
 - No enhancements will be considered for this version
 - A consolidated prioritized list of Errata will be generated by SV Errata Tech-sub-group
 - Errata list will be based on actual faults and difficulties faced by users and/or EDA
 - Errata list will be ratified (including priority and resolutions) by P1800 SV WG
 - Errata prioritization completed by the 9/13 meeting
 - Errata list cataloged by mid Sep
 - Errata received following the deadline will be cataloged and services in future revisions

P1800 Objectives – long term

- Maintain proper alignment and coherence between IEEE SystemVerilog and Verilog language
 - Users don't want to have conflicting usage between SystemVerilog and Verilog
 - IEEE release of SV should enable integration of Verilog in the long run
 - Potential extensions of Verilog constructs to resolve inconsistencies between the two languages that would gate future integration

Accellera Technical Committees

- Keep the four technical committees (1800 {ac, bc, cc, ec}) operational:
 - These are structured to cover the main four language “categories” of Design Modeling, Test Bench, Assertions and DPI
 - Current processes are sufficient in resolving any cross-dependencies between the four sub-committees
 - No need to “merge” these four activities into one group
 - People skills and interest may often be different
 - Maintain current operational process for technical work, in terms of meetings, membership, errata, voting, etc.

Accellera Technical Committees

- SystemVerilog Technical Committees will resolve Errata issues operating under IEEE rules reporting into P1800 Sub Group chaired by the elected nominee
- We encourage the active participation and commitment of SystemVerilog champions in the technical committees

SystemVerilog IEEE LRM

- Appoint an LRM manager who:
 - Places the resolved Errata into the LRM
 - Is responsible on the publication of the drafts
 - Ensures the LRM adheres to the LRM style
 - Monitors and Reports the progress of LRM Editor
- Do we form a small LRM sub-group to help the LRM manager?

P1800 SystemVerilog WEB

- Secretary will be responsible on this
- The P1800 WEB should reflect status, progress and updates made by the group
 - Meeting minutes; agenda; future meetings
 - Project time line and status
 - Procedures & Policies
 - Errata list and Status
 - LRM Drafts
 - Etc.

1364 Technical Committees

- ETF:
 - Maintain committee work for Verilog Errata and make it a SUB-WG for P1800
 - Open nominations for a chair
- BTF & PTF:
 - Need to better understand the work done by these committee (Data Types, Encryption, and PLI) and its future alignment to SystemVerilog
 - Form a small group to report back to P1800 on:
 - Work that was done
 - How it relates to SystemVerilog; conflicts; etc
 - Proposal of merge/adoption into SystemVerilog

➔ Pending Ratification of Modified PAR by NesCom