Make “verification statement” an LRM special term.

Aligned with p1800-2008-draft 4

Objectives: make the term “verification statement” an LRM term, meaning, italicized it where it defined and add it to the glossary.

Modify, the text in blue should be italicized.

16.14 Concurrent assertions

A property on its own is never evaluated for checking an expression. It must be used within a *verification statement* for this to occur. A *verification statement* states the verification function to be performed on the property. The statement can be one of the following:

— **`assert`** to specify the property as a checker to ensure that the property holds for the design
— **`assume`** to specify the property as an assumption for the environment
— **`cover`** to monitor the property evaluation for coverage

Replace

Verilog: The hardware description language (HDL) in IEEE Std 1364-2005.
NOTE—See Clause 2 for information about IEEE Std 1364-2005.

with

Verification statement: A verification statement states the verification function to be performed on the property. The statement can be one of the following:
— **`assert`** to specify the property as a checker to ensure that the property holds for the design
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— **`cover`** to monitor the property evaluation for coverage
NOTE—See 16.14 for a discussion of verification statement.

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