

Assertion enhancements for SV-AC							
Item Number	Item Name	Proposer	Type	Enhancement Description	Target Sub-Committee		
1	assume	Steve Meier	Enhance	assume directive for concurrent assertion to be used as environment, random test generation constraint	SV-AC		
2	immed_assume	SV-AC	Enhance	assume directive that must hold for all times (assumed immediate) alignment/ synchronization with testbench constraints language, clarify on usage/application differences	SV-AC		
3	assume_sync	SV-AC	Enhance	usage/application differences	SV-AC		
4	local_var_ext	John, Bassam	Enhance	local variable reference outside of containing assertion	SV-AC		
5	temp_operators	SV-AC	Enhance	allow additional temporal operators for increased expressivness (omega regular language)	SV-AC		
6	clock_var_assign	Surrendra	Enhance	non-blocking clocked assignment	SV-AC		
7	clock_var_debug	Adam Krolnick	Enhance	debug sampled variable assignments	SV-AC		
8	param_asserts	Joseph Lu	Enhance	support parameters for assertions, extend to allow sequence as parameter	SV-AC		
9	seq_param_module	Adam Krolnick	Enhance	extend module to support sequences to be passed as parameter	SV-AC		
10	inf_pass_argument	Surrendra	Enhance	allow passing of infinite range as argument to properties and sequences	SV-AC		
11	formal_features	Roy Armoni	Enhance	more formal features (TBD)	SV-AC		
Assertion related enhancements for other sub-comittees							
13	event_temporal	Arturo	Enhance	general clocked event object triggered on completion of assertion, handled similar to other verilog events	SV-BC		
14	expect_temporal	Arturo	Enhance	extend expect (blocking wait) to support wait on in-lined sequence event or named clocked event completion	SV-EC		
15	sample_struct	Arturo	Enhance	extend assertions to be used on members of structs and classes within SV.	SV-BC, SV-EC		
16	embed_struct	Arturo	Enhance	SV-BC - for structs, SV-EC for classes feature to embed assertions within a struct, assertion will be checked in every instantiation of object	SV-EC		
17	embed_class	Arturo	Enhance	feature to embed assertions with a class and assertion will be checked in every instantiation of object	SV-EC		
16	define_tb_assert	Arturo	Enhance	define semantics of assertions on testbench variables, variables come in/out of scope			
Assertions not planned to pursue in v3.1a							
20	template	SV-AC	Enhance	template feature (should be passed to BC)	SV-BC		
21	neg_delay	Prakash/DWG	Enhance	extend time windows to allow negative delays	SV-AC		