

Rev 1.0 **Enhancement List for System Verilog Assertions**
 4/28/2003 10:21 List of unprioritized enhancements for v3.1

Item Number	Proposer	Type	Enhancement Description	Proposal	Proposal Owner
1	Connie	Issue	Alignment of system tasks with OVL library		
2	Steve	Enhance	assume directive for concurrent assertion to be used as environment, random test generation constraint		
3	SV-AC	Enhance	assume directive that must hold for all times (assumed immediate)		
4	SV-AC	Enhance	assume alignment/ synchronization with testbench constraints language		
5	Steve	Enhance	assume bias and distribution constraints to change distribution of random tests		
6	John, Bassam	Enhance	local variable reference outside of assertions		
7	SV-AC	Enhance	template feature (should be passed to EC)		
8	Prakash/DWG	Enhance	extend time windows to allow negative delays		
9	SV-AC	Enhance	allow additional temporal operators for increased expressivness (omega regular language)		