SV-AC Issues List **v0.16** **DATE:**

Key	
	Open
	Closed
	Reopened

To open an issue any member w

If there is consensus in a schedu
Any SV-AC member can reques
part of the same company

Item #	Section	Description Semantics	Status	Raised by
1	Sem1	Sequence Implication Operator	Closed	John H, Cindy E, Adrew S.
1.1	Sem1.1	Next sequence implication	Closed	SV-AC
2	Sem2	Check construct	Closed	Adam K, Bassam, Erich
3	Sem3	initial and never are allowed to co-ocurr as directives but are not compatible	Withdrawn	Cindy, John, Erich
4	Sem4	always is implicit	Closed	Cindy, Erich, Adam
5	Sem5	variable feature that provides for multiple assignments	Open	Cindy, Adam, Bassam
6	Syn1	Remove Unary Delay	Closed	Cindy E, 2nd Erich M and John H.
7	Syn2	Replace Seq with Sequence	Closed	Adam K, Cindy E, Bassam T
8	Syn3	true keyword be dropped	Closed	Adam K, Cindy E, Bassam T
9	Syn4	define an implication operator where the rhs will start one cycle later than lhs	closed	Cindy E, 2nd Erich M, John H
10	Syn5	change delay operator semantic	closed	Cindy, 2nd Erich, Bassam
11	Syn7	remove named boolean feature	closed	Cindy, Erich, Adam
12	DWG Syntax	operator syntax (&, |)	Closed	Cindy, Erich, Adam

13	DWG Syntax	never directive	Closed	John, Roy, Cindy
14	DWG Syntax	Issue 1.1 Syntax needs to be addressed	Open	
15	Sem6	Multiple Clocks Support	Open	Joseph Lu, Roy, Hillel
16	Sem7	Always is explicitly reqd only at declarative level and initial and always is not allowed at proc level	Open	Cindy E, John H, Jospeh Lu
17	Sem8	Allow negation of rhs sequence of implication	Open	John, Surrendra, Roy
18	Syntax group	Clarification on templates	Open	John, Surrendra, Roy
19	Sem8	new built in operator for next_event	Open	Adam, Surrendra, John

3-Mar-03

ıith two seconds. A written description of the issue is required

ıled SV-AC meeting or issue has been voted upon
t an issue to be reopened must have two seconds from other members who are not

Description	Resolution
John and Surrendra submitted proposals. Surrendra's proposal is current.	
Issue whether nesting of sequence implication should be supported to enabled variable sampling.	Syntax
Remove immediate assertions. Proposal is self evident. Prakash presented arguments for preserving.	Failed
Do not allow intial and never to occur in same property. Proposal is self evident.	Withdrawn
Require always as keyword to be explicit and that one of {always, never} be required for correct syntax. Proposal is self evident	Passed DWG syntax
Cindy will provide proposal	
Proposals are combined with issue #10. 1 proposal by Cindy, 2nd proposal by Surrendra	Stay as is in LRM
Replace seq with sequence	Replace seq with sequence. No dissent
	Remove true keyword or use 1
Cindy proposal to add additional sequence implication operator that is non-overlapping. Adam has proposal to change sequence implication to the non-overlapping type	Passed DWG syntax
proposal by Cindy to have two different bind operators - see email (combine with issue 6 Syn1). Surrendra proposal	No change to LRM
remove feature to define bool	remove from LRM
Proposals from Cindy and Roy on using various symbols to represent sequence operators	Using && for "and", || for "or" and keyword "intersect" is preserved.

Proposal from John to change never directive to not to match semantic meaning.	Changed to not (by consensus)
Replace prop_expr in implication production with seq_expr. John and Surrendra to create BNF for named formulas.	Need BNF change
John Havilecek proposal by email	
disallow prop. expr. inside proc. code.	
email proposal from John. Allow not after sequence implication	
Adam will send list of requirements	